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(71) Applicant: **AMBERWAVE SYSTEMS CORPORATION** [US/US]; 13 Garabedian Drive, Salem, NH 03079 (US).

(72) Inventors: **LOCHTEFELD, Anthony, J.**; 73 Garrison Avenue, Somerville, MA 02144 (US). **LANGDO, Thomas, A.**; 195 Binney Street, Apt. 4302, Cambridge, MA 02142 (US). **HAMMOND, Richard**; 55 Sands Road, Harriseahead, Stoke-on-Trent, Staffordshire England ST74JZ (GB). **CURRIE, Matthew, T.**; 8 Fletcher Road, Windham, NH 03087 (US). **BRAITHWAITE, Glyn**; 1465 Hooksett Road, #186, Hooksett, NH 03106 (US). **FITZGERALD, Eugene, A.**; 7 Camelot Road, Windham, NH 03087 (US).

(74) Agent: **NATASHA, C.**; Testa, Hurwitz & Thibeault, LLP, High Street Tower, 125 High Street, Boston, MA 02110 (US).

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(54) Title: STRAINED-SEMICONDUCTOR-ON-INSULATOR DEVICE STRUCTURES

(57) Abstract: The benefits of strained semiconductors are combined with silicon-on-insulator approaches to substrate and device fabrication.

STRAINED-SEMICONDUCTOR-ON-INSULATOR DEVICE STRUCTURES

Related Applications

This application claims the benefit of U.S. Provisional Application 60/386,968 filed June 7, 2002, U.S. Provisional Application 60/404,058 filed August 15, 2002, and U.S. Provisional Application 60/416,000 filed October 4, 2002; the entire disclosures of these three provisional applications are hereby incorporated by reference

Field of the Invention

This invention relates to devices and structures comprising strained semiconductor layers and insulator layers.

Background

Strained silicon-on-insulator structures for semiconductor devices combine the benefits of two advanced approaches to performance enhancement: silicon-on-insulator (SOI) technology and strained silicon (Si) technology. The strained silicon-on-insulator configuration offers various advantages associated with the insulating substrate, such as reduced parasitic capacitances and improved isolation. Strained Si provides improved carrier mobilities. Devices such as strained Si metal-oxide-semiconductor field-effect transistors (MOSFETs) combine enhanced carrier mobilities with the advantages of insulating substrates.

Strained-silicon-on-insulator substrates are typically fabricated as follows. First, a relaxed silicon-germanium (SiGe) layer is formed on an insulator by one of several techniques such as separation by implantation of oxygen (SIMOX), wafer bonding and etch back; wafer bonding and hydrogen exfoliation layer transfer; or recrystallization of amorphous material. Then, a strained Si layer is epitaxially grown to form a strained-silicon-on-insulator structure, with strained Si disposed over SiGe. The relaxed-SiGe-on-insulator layer serves as the template for inducing strain in the Si layer. This induced strain is typically greater than 10^{-3}.

This structure has limitations. It is not conducive to the production of fully-depleted strained-semiconductor-on-insulator devices in which the layer over the insulating material must be thin enough [<300 angstroms (Å)] to allow for full depletion of the layer during device operation. Fully depleted transistors may be the favored version of SOI for MOSFET

technologies beyond the 90 nm technology node. The relaxed SiGe layer adds to the total thickness of this layer and thus makes it difficult to achieve the thicknesses required for fully depleted silicon-on-insulator device fabrication. The relaxed SiGe layer is not required if a strained Si layer can be produced directly on the insulating material. Thus, there is a need for a method to produce strained silicon – or other semiconductor – layers directly on insulating substrates.

Double-gate MOSFETs

Double gate MOSFETs have the potential for superior performance in comparison to standard single-gate bulk or single-gate SOI MOSFET devices. This is due to the fact that two gates (one above and one below the channel) allow much greater control of channel charge then a single gate. This configuration has the potential to translate to higher drive current and lower stand-by leakage current.

finFETs

Fin-field-effect transistors (finFETs), like double-gate MOSFETs, typically have two gates (one on either side of the channel, where the channel is here oriented vertically) allowing much greater control of channel charge than in a single gate device. This configuration also has the potential to translate to higher drive current and lower stand-by leakage current. Devices related to the finFET, such as the wrap-around gate FET (gate on both sides of as well as above the channel) allow even more channel charge control and hence even more potential for improved drive current and leakage current performance.

Bipolar-CMOS

The bipolar-CMOS (BiCMOS) process is a combination of both the bipolar transistor and MOSFET/CMOS processes. Individually, the CMOS process allows low power dissipation, high packing density and the ability to integrate complexity with high-speed yields. A major contribution to power dissipation in CMOS circuits originates from driving the load capacitance that is usually the gate of sequentially linked logic cells. The size of these gates may be kept sufficiently small, but when driving higher loads (such as input/output buffers or data buses) the load or capacitance of such devices is substantially larger and therefore requires greater gate width (hence area) of transistor, which inevitably drives down the switching speed of the MOSFET.

The bipolar transistor has significant advantages in terms of the drive current per unit active area and reduced noise signal. Additionally, the switching speed is enhanced due to the

effectively exponential output current swing with respect to input signal. This means that the transconductance of a bipolar transistor is significantly higher than that of a MOS transistor when the same current is passed. Higher transconductance enables the charging process to take place approximately ten times more quickly in emitter coupled logic circuits, or high fan out/load capacitance.

Pure bipolar technology has not replaced the high packing density microprocessor CMOS process for a number of reasons, including issues of yield and the increased area required for device isolation. However, integration of bipolar and CMOS may provide the best aspects of the composite devices.

The advantages of BiCMOS process may be summarized as follows:

1. Improved speed performance of highly integrated functionality of CMOS technology;
2. Lower power dissipation than bipolar technology;
3. Lower sensitivity to fan out and capacitive load;
4. Increased flexibility of input/output interface;
5. Reduced clock skew;
6. Improved internal gate delay; and
7. Reduced need for aggressive scaling because a 1 - 2 μm BiCMOS process offers circuit speed equivalent to that of sub-micron CMOS.

Summary

The present invention includes a strained-semiconductor-on-insulator (SSOI) substrate structure and methods for fabricating the substrate structure. MOSFETs fabricated on this substrate will have the benefits of SOI MOSFETs as well as the benefits of strained Si mobility enhancement. For example, the formation of BiCMOS structures on SSOI substrates provides the combined benefits of BiCMOS design platforms and enhanced carrier mobilities. SSOI substrates also enable enhanced carrier mobilities, process simplicity, and better device isolation for double-gate MOSFETs and finFETs.

By eliminating the SiGe relaxed layer traditionally found beneath the strained Si layer, the use of SSOI technology is simplified. For example, issues such as the diffusion of Ge into the strained Si layer during high temperature processes are avoided.

This approach enables the fabrication of well-controlled, epitaxially-defined, thin strained semiconductor layers directly on an insulator layer. Tensile strain levels of $\sim 10^{-3}$ or greater are

possible in these structures, and are not diminished after thermal anneal cycles. In some embodiments, the strain-inducing relaxed layer is not present in the final structure, eliminating some of the key problems inherent to current strained Si-on-insulator solutions. This fabrication process is suitable for the production of enhanced-mobility substrates applicable to partially or fully depleted SSOI technology.

In an aspect, the invention features a structure that includes a first substrate having a dielectric layer disposed thereon, and a first strained semiconductor layer disposed in contact with the dielectric layer.

One or more of the following features may be included. The strained semiconductor layer may include at least one of a group II, a group III, a group IV, a group V, and a group VI element, such as silicon, germanium, silicon germanium, gallium arsenide, indium phosphide, or zinc selenide. The strained semiconductor layer may be substantially free of germanium, and any other layer disposed in contact with the strained semiconductor layer may be substantially free of germanium. The strained semiconductor layer may be tensilely strained or compressively strained. The strained semiconductor layer may have a strained portion and a relaxed portion.

A second strained semiconductor layer may be in contact with the first strained semiconductor layer. The first strained semiconductor layer may be compressively strained and the second strained semiconductor layer may be tensilely strained, or vice versa.

The structure may include a transistor having a source region and a drain region disposed in a portion of the strained semiconductor layer, a gate disposed above the strained semiconductor layer and between the source and drain regions, and a gate dielectric layer disposed between the gate and the strained semiconductor layer.

The strained semiconductor layer may have been formed on a second substrate, may have been disposed in contact with the dielectric layer by bonding, and may have a lower dislocation density than an initial dislocation density of the strained semiconductor layer as formed. The initial dislocation density may have been lowered by etching. The strained semiconductor layer may have been grown with an initial dislocation density and may have a dislocation density less than the initial dislocation density. The strained semiconductor layer may have been formed by epitaxy. The strained semiconductor layer may have a thickness uniformity of better than approximately ±5%. The strained layer has a thickness selected from a range of approximately 20 angstroms - 1000 angstroms. The strained layer has a surface roughness of less than approximately 20 angstroms. The substrate may include silicon and/or germanium.

In another aspect, the invention features a structure including a relaxed substrate including a bulk material, and a strained layer disposed in contact with the relaxed substrate. The strain of the strained layer is not induced by the underlying substrate, and the strain is independent of a lattice mismatch between the strained layer and the relaxed substrate. The bulk material may include a first semiconductor material. The strained layer may include a second semiconductor material. The first semiconductor material may be essentially the same as the second semiconductor material. The first and second semiconductor material may include silicon. A lattice constant of the relaxed substrate may be equal to a lattice constant of the strained layer in the absence of strain. The strain of the strained layer may be greater than approximately 1×10^{-3}. The strained layer may have been formed by epitaxy. The strained layer may have a thickness uniformity of better than approximately ±5%. The strained layer may have a thickness selected from a range of approximately 20 angstroms - 1000 angstroms. The strained layer may have a surface roughness of less than approximately 20 angstroms.

The structure may include a transistor having a source region and a drain region disposed in a portion of the strained semiconductor layer, a gate contact disposed above the strained semiconductor layer and between the source and drain regions, and a gate dielectric layer disposed between the gate contact and the strained semiconductor layer.

In another aspect, the invention features a structure including a substrate including a dielectric material, and a strained semiconductor layer disposed in contact with the dielectric material.

One or more of the following features may be included. The dielectric material may include sapphire. The semiconductor layer may have been formed on a second substrate, have been disposed in contact with the dielectric material by bonding, and have a lower dislocation density than an initial dislocation density of the semiconductor layer as formed. The initial dislocation density may have been lowered by etching. The semiconductor layer may have been formed by epitaxy.

In another aspect, the invention features a method for forming a structure, the method including providing a first substrate having a first strained semiconductor layer formed thereon, bonding the first strained semiconductor layer to an insulator layer disposed on a second substrate and, removing the first substrate from the first strained semiconductor layer, the strained semiconductor layer remaining bonded to the insulator layer.

One or more of the following features may be included. The strained semiconductor layer may be tensilely or compressively strained. The strained semiconductor layer may include a surface layer or a buried layer after the removal of the first substrate.

Removing the first substrate from the strained semiconductor layer may include cleaving. Cleaving may include implantation of an exfoliation species through the strained semiconductor layer to initiate cleaving. The exfoliation species may include at least one of hydrogen and helium. Providing the first substrate may include providing the first substrate having a second strained layer disposed between the substrate and the first strained layer, the second strained layer acting as a cleave plane during cleaving. The second strained layer may include a compressively strained layer. The compressively strained layer may include $Si_{1-x}Ge_x$. The first substrate may have a relaxed layer disposed between the substrate and the first strained layer.

The relaxed layer may be planarized prior to forming the first strained semiconductor layer. After the relaxed layer is planarized, a relaxed semiconductor regrowth layer may be formed thereon. A dielectric layer may be formed over the first strained semiconductor layer prior to bonding the first strained semiconductor layer to an insulator layer. Removing the first substrate from the strained semiconductor layer may include mechanical grinding. Bonding may include achieving a high bond strength, e.g., greater than or equal to about 1000 milliJoules/meter squared (mJ/m^2), at a low temperature, e.g., less than approximately 600 °C.

Bonding may include plasma activation of a surface of the first semiconductor layer prior to bonding the first semiconductor layer. Plasma activation may include use of at least one of an ammonia (NH_3), an oxygen (O_2), an argon (Ar), and a nitrogen (N_2) source gas. Bonding may include planarizing a surface of the first semiconductor layer prior to bonding the first semiconductor layer by, e.g., chemical-mechanical polishing. A portion of the first strained semiconductor layer may be relaxed such as by, e.g., introducing a plurality of ions into the portion of the first strained semiconductor layer.

A transistor may be formed by forming a gate dielectric layer above a portion of the strained semiconductor layer, forming a gate contact above the gate dielectric layer, and forming a source region and a drain region in a portion of the strained semiconductor layer, proximate the gate dielectric layer.

In another aspect, the invention features a method for forming a structure, the method including providing a substrate having a relaxed layer disposed over a first strained layer, the

relaxed layer inducing strain in the first strained layer, and removing at least a portion of the relaxed layer selectively with respect to the first strained layer.

One or more of the following features may be included. The first strained layer may be bonded to the substrate, including, e.g., to an insulator layer disposed on the substrate. The first strained layer may be formed over the relaxed layer on another substrate. The portion of the relaxed layer may be removed by, e.g., oxidation, a wet chemical etch, a dry etch, and/or chemical-mechanical polishing. After removal of at least a portion of the relaxed layer, the strained layer may be planarized by, e.g., chemical-mechanical polishing and/or an anneal. The anneal may be performed at a temperature greater than 800 °C.

The substrate may have an etch stop layer disposed between the relaxed layer and the strained layer. The etch stop layer may be compressively strained. The strained layer may include silicon, the relaxed layer may include silicon germanium, and the etch stop layer may include silicon germanium carbon. The relaxed layer may include $Si_{1-y}Ge_y$, the etch stop layer may include $Si_{1-x}Ge_x$, and x may be greater than y, e.g., x may be approximately 0.5 and y may be approximately 0.2. The etch stop layer enables an etch selectivity to the relaxed layer of greater than 10:1, e.g., greater than 100:1. The etch stop layer may have a thickness selected from a range of about 20 angstroms to about 1000 angstroms. The relaxed layer may be formed over a graded layer.

In another aspect, the invention features a method for forming a structure, the method including providing a first substrate having a dielectric layer disposed thereon, and forming a semiconductor layer on a second substrate, the semiconductor layer having an initial misfit dislocation density. The semiconductor layer is bonded to the dielectric layer, and the second substrate is removed, the semiconductor layer remaining bonded to the dielectric layer. The misfit dislocation density in the semiconductor layer is reduced.

One or more of the following features may be included. The misfit dislocation density may be reduced by removing a portion of the semiconductor layer, such as, e.g., by etching. After removing a portion of the semiconductor layer to reduce misfit dislocation density, a regrowth layer may be formed over the semiconductor layer without increasing misfit dislocation density. The regrowth layer may be formed by epitaxy.

In another aspect, the invention features a method for forming a structure, the method including providing a first substrate having a dielectric layer disposed thereon, forming a semiconductor layer on a second substrate, the semiconductor layer having an initial misfit

dislocation density. The semiconductor layer is bonded to the dielectric layer. The second substrate is removed, the semiconductor layer remaining bonded to the dielectric layer, and a regrowth layer is grown over the semiconductor layer.

One or more of the following features may be included. The semiconductor layer and the regrowth layer may include the same semiconductor material. The semiconductor layer and the regrowth layer together may have a misfit dislocation density not greater than the initial misfit dislocation density.

In another aspect, the invention features a method for forming a structure, the method including providing a first substrate having a strained layer disposed thereon, the strained layer including a first semiconductor material, and bonding the strained layer to a second substrate, the second substrate including a bulk material. The first substrate is removed from the strained layer, the strained layer remaining bonded to the bulk semiconductor material. The strain of the strained layer is not induced by the second substrate and the strain is independent of lattice mismatch between the strained layer and the second substrate.

One or more of the following features may be included. The bulk material may include a second semiconductor material. The first semiconductor material may be substantially the same as the second semiconductor material. The second substrate and/or the strained semiconductor layer may include silicon.

In another aspect, the invention features a method for forming a structure, the method including providing a first substrate having a semiconductor layer disposed over a strained layer. The semiconductor layer is bonded to an insulator layer disposed on a second substrate, and the first substrate is removed from the strained layer, the semiconductor layer remaining bonded to the insulator layer.

One or more of the following features may be included. The semiconductor layer may be substantially relaxed. The semiconductor layer and/or the strained layer may include at least one of a group II, a group III, a group IV, a group V, and a group VI element. The semiconductor layer may include germanium and the strained layer may include silicon.

In another aspect, the invention features a structure including a substrate having a dielectric layer disposed thereon; and a strained semiconductor layer disposed in contact with the dielectric layer, the semiconductor layer including approximately 100% germanium.

One or more of the following features may be included. The strained semiconductor layer may be compressively strained. The strained semiconductor layer may include a thin layer

and the thin layer is disposed in contact with the dielectric layer. The thin layer may include silicon.

In another aspect, the invention features a substrate having a dielectric layer disposed thereon, a strained semiconductor layer disposed in contact with the dielectric layer, and a transistor. The transistor includes a source region and a drain region disposed in a portion of the strained semiconductor layer, and a gate disposed above the strained semiconductor layer and between the source and drain regions, the gate including a material selected from the group consisting of a doped semiconductor, a metal, and a metallic compound.

One or more of the following features may be included. The doped semiconductor may include polycrystalline silicon and/or polycrystalline silicon-germanium. The metal may include titanium, tungsten, molybdenum, tantalum, nickel, and/or iridium. The metal compound may include titanium nitride, titanium silicon nitride, tungsten nitride, tantalum nitride, tantalum silicide, nickel silicide, and/or iridium oxide. A contact layer may be disposed over at least a portion of the strained semiconductor layer, with a bottommost boundary of the contact layer being disposed above a bottommost boundary of the strained semiconductor layer. The contact layer may share an interface with the semiconductor layer.

In another aspect, the invention features a structure including a substrate having a dielectric layer disposed thereon, the dielectric layer having a melting point greater than about 1700°C, and a strained semiconductor layer disposed in contact with the dielectric layer.

The following features may be included. The dielectric layer may include aluminum oxide, magnesium oxide, and/or silicon nitride.

In another aspect, the invention features a structure including a substrate having a dielectric layer disposed thereon; and a strained semiconductor layer disposed in contact with the dielectric layer. The strained semiconductor layer includes approximately 100% silicon and has a misfit dislocation density of less than about 10^5 cm/cm^2.

In another aspect, the invention features a structure including a substrate having a dielectric layer disposed thereon, and a strained semiconductor layer disposed in contact with the dielectric layer. The strained semiconductor layer includes approximately 100% silicon and has a threading dislocation density selected from the range of about 10 dislocations/cm^2 to about 10^7 dislocations/cm^2.

In another aspect, the invention features a structure including a substrate having a dielectric layer disposed thereon and a strained semiconductor layer disposed in contact with the

dielectric layer. The semiconductor layer includes approximately 100% silicon and has a surface roughness selected from the range of approximately 0.01 nm to approximately 1 nm.

In another aspect, the invention features a substrate having a dielectric layer disposed thereon, and a strained semiconductor layer disposed in contact with the dielectric layer. The strained semiconductor layer includes approximately 100% silicon and has a thickness uniformity across the substrate of better than approximately ±10%.

In another aspect, the invention features a structure including a substrate having a dielectric layer disposed thereon, and a strained semiconductor layer disposed in contact with the dielectric layer. The strained semiconductor layer includes approximately 100% silicon and has a thickness of less than approximately 200 Å.

In another aspect, the invention features a structure including a substrate having a dielectric layer disposed thereon, and a strained semiconductor layer disposed in contact with the dielectric layer. The semiconductor layer includes approximately 100% silicon and has a surface germanium concentration of less than approximately $1x10^{12}$ atoms/cm^2

In another aspect, the invention features a structure including a substrate having a dielectric layer disposed thereon, and a strained semiconductor layer disposed in contact with the dielectric layer. An interface between the strained semiconductor layer and the dielectric layer has a density of bonding voids of less than 0.3 voids/cm^2.

In another aspect, the invention features a method for forming a structure, the method including providing a first substrate comprising a porous layer defining a cleave plane and having a first strained semiconductor layer formed thereon. The first strained semiconductor layer is bonded to an insulator layer disposed on a second substrate, and removing the first substrate from the first strained semiconductor layer by cleaving at the cleave plane, the strained semiconductor layer remaining bonded to the insulator layer.

In another aspect, the invention features a method for forming a structure, the method including forming a first relaxed layer over a first substrate, the first relaxed layer including a porous layer defining a cleave plane. A strained semiconductor layer is formed over the first relaxed layer. The first strained semiconductor layer is bonded to an insulator layer disposed on a second substrate. The first substrate is removed from the strained semiconductor layer by cleaving at the cleave plane, the strained semiconductor layer remaining bonded to the insulator layer

One or more of the following features may be included. The porous layer may be disposed at a top portion of the first relaxed layer. A second relaxed layer may be formed over the first relaxed layer, with the strained semiconductor layer being formed over the second relaxed layer. The first relaxed layer may be planarized, e.g., by chemical-mechanical polishing, prior to forming the second relaxed layer. At least a portion of the porous layer may remain disposed on the first strained semiconductor layer after cleaving. The portion of the porous layer may be removed from the strained semiconductor layer after cleaving. The portion of the porous layer may be removed by cleaning with a wet chemical solution that may include, e.g., hydrogen peroxide and/or hydrofluoric acid. Removing the portion of the porous layer may include oxidation.

In another aspect, the invention features a structure including a substrate having a dielectric layer disposed thereon and a fin-field-effect transistor disposed over the substrate. The fin-field-effect-transistor includes a source region and a drain region disposed in contact with the dielectric layer, the source and the drain regions includinga strained semiconductor material. The fin-field-effect-transistor also includes at least one fin extending between the source and the drain regions, the fin including a strained semiconductor material. A gate is disposed above the strained semiconductor layer, extending over at least one fin and between the source and the drain regions. A gate dielectric layer is disposed between the gate and the fin.

One or more of the following features may be included. The fin may include at least one of a group II, a group III, a group IV, a group V, of a group VI element. The strained semiconductor layer may be tensilely strained and may include, e.g., tensilely strained silicon. The strained semiconductor layer may be compressively strained and may include, e.g., compressively strained germanium.

In another aspect, the invention features a method for forming a structure, the method including providing a substrate having a dielectric layer disposed thereon, and a first strained semiconductor layer disposed in contact with the dielectric layer. A fin-field-effect transistor is formed on the substrate by patterning the first strained semiconductor layer to define a source region, a drain region, and at least one fin disposed between the source and the drain regions. A dielectric layer is formed, at least a portion of the dielectric layer being disposed over the fin, and a gate is formed over the dielectric layer portion disposed over the fin.

One or more of the following features may be included. The first strained semiconductor layer may include at least one of a group II, a group III, a group IV, a group V, or a group VI

element. The strained semiconductor layer may be tensilely strained and may include, e.g., tensilely strained silicon. The strained semiconductor layer may be compressively strained and may include, e.g., compressively strained germanium.

In another aspect, the invention features a structure including a dielectric layer disposed over a substrate; and a transistor formed over the dielectric layer. The transistor includes a first gate electrode in contact with the dielectric layer, a strained semiconductor layer disposed over the first gate electrode; and a second gate electrode disposed over the strained semiconductor layer.

One or more of the following features may be included. The strained semiconductor layer may include at least one of a group II, a group III, a group IV, a group V, and a group VI elements.

The strained semiconductor layer may be tensilely strained and may include, e.g., tensilely strained silicon. The strained semiconductor layer may be compressively strained and may include, e.g., compressively strained germanium. The strained semiconductor layer may have a strain level greater than 10^{-3}.

A first gate insulator layer may be disposed between the first gate electrode and the strained semiconductor layer. A second gate insulator layer may be disposed between the strained semiconductor layer and the second gate electrode. The strained semiconductor layer may include a source. The strained semiconductor layer may include a drain. A sidewall spacer may be disposed proximate the second gate electrode. The sidewall spacer may include a dielectric or a conductive material.

In another aspect, the invention features a method for forming a structure, the method including forming a substrate having a first gate electrode layer disposed over a substrate insulator layer, a first gate insulator layer disposed over the first gate electrode layer, and a strained semiconductor layer disposed over the first gate insulator layer. A second gate insulator layer is formed over the strained semiconductor layer, and a second gate electrode layer is formed over the second gate insulator layer. A second gate electrode is defined by removing a portion of the second gate insulator layer. A dielectric sidewall spacer is formed proximate the second gate electrode. A portion of the strained semiconductor layer, a portion of the first gate insulator layer, and a portion of the first gate electrode layer are removed to define a vertical structure disposed over the substrate insulator layer, the vertical structure including a strained layer region, a first gate insulator region, and a first gate electrode layer region disposed under

the second gate electrode. A first gate electrode is defined by laterally shrinking the first gate electrode layer region.

One or more of the following features may be included. The strained semiconductor layer may be tensilely strained and may include, e.g., tensilely strained silicon. The strained semiconductor layer may be compressively strained and may include compressively strained germanium. A conductive sidewall spacer may be formed proximate the dielectric sidewall spacer. A source and/or a drain may be defined in the strained semiconductor layer.

In another aspect, the invention features a structure including a strained semiconductor layer disposed over a dielectric layer and a bipolar transistor. The bipolar transistor includes a collector disposed in a portion of the strained semiconductor layer, a base disposed over the collector, and an emitter disposed over the base.

One or more of the following features may be included. The strained layer may be tensilely strained and may include, e.g., tensilely strained silicon. The strained layer may be compressively strained.

In another aspect, the invention features a relaxed substrate including a bulk material, a strained layer disposed in contact with the relaxed substrate; and a bipolar transistor. The bipolar transistor includes a collector disposed in a portion of the strained layer, a base disposed over the collector, and an emitter disposed over the base. The strain of the strained layer is not induced by the underlying substrate.

One or more of the following features may be included. The strained layer may be tensilely strained and may include, e.g., tensilely strained silicon. The strained layer may be compressively strained.

In another aspect, the invention features a structure including a relaxed substrate including a bulk material, a strained layer disposed in contact with the relaxed substrate; and a bipolar transistor including. The bipolar transistor includes a collector disposed in a portion of the strained layer, a base disposed over the collector, and an emitter disposed over the base. The strain of the strained layer is independent of a lattice mismatch between the strained layer and the relaxed substrate.

One or more of the following features may be included. The strained layer may be tensilely strained and may include, e.g., tensilely strained silicon. The strained layer may be compressively strained.

In another aspect, the invention includes a method for forming a structure, the method including providing a substrate having a strained semiconductor layer disposed over a dielectric layer, defining a collector in a portion of the strained semiconductor layer; forming a base over the collector; and forming an emitter over the base.

One or more of the following features may be included. The strained layer may be tensilely strained and may include, e.g., tensilely strained silicon. The strained layer may be compressively strained.

In another aspect, the invention includes method for forming a structure, the method including providing a first substrate having a strained layer disposed thereon, the strained layer including a first semiconductor material. The strained layer is bonded to a second substrate, the second substrate including a bulk material. The first substrate is removed from the strained layer, with the strained layer remaining bonded to the bulk semiconductor material. A collector is defined in a portion of the strained layer. A base is formed over the collector; and an emitter is formed over the base. The strain of the strained layer is not induced by the second substrate and the strain is independent of lattice mismatch between the strained layer and the second substrate.

One or more of the following features may be included. The strained layer may be tensilely strained and may include, e.g., tensilely strained silicon. The strained layer may be compressively strained.

In another aspect, the invention features a method for forming a structure, the method including providing a relaxed substrate comprising a bulk material and a strained layer disposed in contact with the relaxed substrate, the strain of the strained layer not being induced by the underlying substrate and the strain being independent of a lattice mismatch between the strained layer and the relaxed substrate. A collector is defined in a portion of the strained layer. A base is formed over the collector, and an emitter is formed over the base.

One or more of the following features may be included. The strained layer may be tensilely strained and may include, e.g., tensilely strained silicon. The strained layer may be compressively strained.

In another aspect, the invention features a method for forming a structure, the method includes providing a substrate having a strained semiconductor layer disposed over a substrate dielectric layer and forming a transistor in the strained layer. Forming the transistor includes forming a gate dielectric layer above a portion of the strained semiconductor layer, forming a gate contact above the gate dielectric layer, and forming a source region and a drain region in a

portion of the strained semiconductor layer, proximate the gate dielectric layer. A portion of the strained layer and the substrate dielectric layer are removed to expose a portion of the substrate. A collector is defined in the exposed portion of the substrate. A base is formed over the collector; and an emitter is formed over the base.

One or more of the following features may be included. The strained layer may be tensilely strained and may include, e.g., tensilely strained silicon. The strained layer may be compressively strained.

Brief Description of Drawings

Figures 1A - 6 are schematic cross-sectional views of substrates illustrating a method for fabricating an SSOI substrate;

Figure 7 is a schematic cross-sectional view illustrating an alternative method for fabricating the SSOI substrate illustrated in Figure 6;

Figure 8 is a schematic cross-sectional view of a transistor formed on the SSOI substrate illustrated in Figure 6;

Figures 9 - 10 are schematic cross-sectional views of substrate(s) illustrating a method for fabricating an alternative SSOI substrate;

Figure 11 is a schematic cross-sectional view of a substrate having several layers formed thereon;

Figures 12 - 13 are schematic cross-sectional views of substrates illustrating a method for fabricating an alternative strained semiconductor substrate;

Figure 14 is a schematic cross-sectional view of the SSOI substrate illustrated in Figure 6 after additional processing;

Figures 15 - 21B are cross-sectional and top views of substrates illustrating a method for fabricating a fin-field-effect transistor (finFET) on an SSOI substrate;

Figures 22 - 35 are cross-sectional views of substrates illustrating a method for fabricating a dual-gate transistor on an SSOI substrate;

Figures 36 - 39 are cross-sectional views of substrates illustrating a method for fabricating a bipolar transistor on an SSOI substrate; and

Figures 40A - 41D are schematic cross-sectional views of substrates illustrating alternative methods for fabricating an SSOI substrate.

Like-referenced features represent common features in corresponding drawings.

Detailed Description

An SSOI structure may be formed by wafer bonding followed by cleaving. Figures 1A - 2B illustrate formation of a suitable strained layer on a wafer for bonding, as further described below.

Referring to Figure 1A, an epitaxial wafer 8 has a plurality of layers 10 disposed over a substrate 12. Substrate 12 may be formed of a semiconductor, such as Si, Ge, or SiGe. The plurality of layers 10 includes a graded buffer layer 14, which may be formed of $Si_{1-y}Ge_y$, with a maximum Ge content of, e.g., 10 - 80% (i.e., y = 0.1 - 0.8) and a thickness T_1 of, for example, 1 - 8 micrometers (μm).

A relaxed layer 16 is disposed over graded buffer layer 14. Relaxed layer 16 may be formed of uniform $Si_{1-x}Ge_x$ having a Ge content of, for example, 10 - 80 % (i.e., x = 0.1 - 0.8), and a thickness T_2 of, for example, 0.2 - 2 μm. In some embodiments, $Si_{1-x}Ge_x$ may include $Si_{0.70}Ge_{0.30}$ and T_2 may be approximately 1.5 μm. Relaxed layer 16 may be fully relaxed, as determined by triple axis X-ray diffraction, and may have a threading dislocation density of <1 x 10^6 dislocations/cm^2, as determined by etch pit density (EPD) analysis. Because threading dislocations are linear defects disposed within a volume of crystalline material, threading dislocation density may be measured as either the number of dislocations intersecting a unit area within a unit volume or the line length of dislocation per unit volume. Threading dislocation density therefore, may, be expressed in either units of dislocations/cm^2 or cm/cm^3. Relaxed layer 16 may have a surface particle density of, e.g., less than about 0.3 particles/cm^2. Further, relaxed layer 16 produced in accordance with the present invention may have a localized light-scattering defect level of less than about 0.3 defects/cm^2 for particle defects having a size (diameter) greater than 0.13 microns, a defect level of about 0.2 defects/cm^2 for particle defects having a size greater than 0.16 microns, a defect level of about 0.1 defects/cm^2 for particle defects having a size greater than 0.2 microns, and a defect level of about 0.03 defects/cm^2 for defects having a size greater than 1 micron. Process optimization may enable reduction of the localized light-scattering defect levels to about 0.09 defects/cm^2 for particle defects having a size greater than 0.09 microns and to 0.05 defects/cm^2 for particle defects having a size greater than 0.12 microns.

Substrate 12, graded layer 14, and relaxed layer 16 may be formed from various materials systems, including various combinations of group II, group III, group IV, group V, and group VI

elements. For example, each of substrate 12, graded layer 14, and relaxed layer 16 may include a III-V compound. Substrate 12 may include gallium arsenide (GaAs), graded layer 14 and relaxed layer 16 may include indium gallium arsenide (InGaAs) or aluminum gallium arsenide (AlGaAs). These examples are merely illustrative, and many other material systems are suitable.

A strained semiconductor layer 18 is disposed over relaxed layer 16. Strained layer 18 may include a semiconductor such as at least one of a group II, a group III, a group IV, a group V, and a group VI element. Strained semiconductor layer 18 may include, for example, Si, Ge, SiGe, GaAs, indium phosphide (InP), and/or zinc selenide (ZnSe). In some embodiments, strained semiconductor layer 18 may include approximately 100% Ge, and may be compressively strained. Strained semiconductor layer 18 comprising 100% Ge may be formed over, e.g., relaxed layer 16 containing uniform $Si_{1-x}Ge_x$ having a Ge content of, for example, 50 - 80 % (i.e., x = 0.5 - 0.8), preferably 70% (x=0.7). Strained layer 18 has a thickness T_3 of, for example, 50 - 1000 Å. In an embodiment, T_3 may be approximately 200 - 500 Å.

Strained layer 18 may be formed by epitaxy, such as by atmospheric-pressure CVD (APCVD), low- (or reduced-) pressure CVD (LPCVD), ultra-high-vacuum CVD (UHVCVD), by molecular beam epitaxy (MBE), or by atomic layer deposition (ALD). Strained layer 18 containing Si may be formed by CVD with precursors such as silane, disilane, or trisilane. Strained layer 18 containing Ge may be formed by CVD with precursors such as germane or digermane. The epitaxial growth system may be a single-wafer or multiple-wafer batch reactor. The growth system may also utilize a low-energy plasma to enhance layer growth kinetics. Strained layer 18 may be formed at a relatively low temperature, e.g., less than 700 °C, to facilitate the definition of an abrupt interface 17 between strained layer 18 and relaxed layer 16. This abrupt interface 17 may enhance the subsequent separation of strained layer 18 from relaxed layer 16, as discussed below with reference to Figures 4 and 5. Abrupt interface 17 is characterized by the transition of Si or Ge content (in this example) proceeding in at least 1 decade (order of magnitude in atomic concentration) per nanometer of depth into the sample. In an embodiment, this abruptness may be better than 2 decades per nanometer.

In an embodiment in which strained layer 18 contains substantially 100% Si, strained layer 18 may be formed in a dedicated chamber of a deposition tool that is not exposed to Ge source gases, thereby avoiding cross-contamination and improving the quality of the interface between strained layer 18 and relaxed layer 16. Furthermore, strained layer 18 may be formed from an isotopically pure silicon precursor(s). Isotopically pure Si has better thermal

conductivity than conventional Si. Higher thermal conductivity may help dissipate heat from devices subsequently formed on strained layer 18, thereby maintaining the enhanced carrier mobilities provided by strained layer 18.

After formation, strained layer 18 has an initial misfit dislocation density, of, for example, 0 - 10^5 cm/cm^2. In an embodiment, strained layer 18 has an initial misfit dislocation density of approximately 0 cm/cm^2. Because misfit dislocations are linear defects generally lying within a plane between two crystals within an area, they may be measured in terms of total line length per unit area. Misfit dislocation density, therefore, may be expressed in units of dislocations/cm or cm/cm^2. In one embodiment, strained layer 18 is tensilely strained, e.g., Si formed over SiGe. In another embodiment, strained layer 18 is compressively strained, e.g., Ge formed over SiGe.

Strained layer 18 may have a surface particle density of, e.g., less than about 0.3 particles/cm^2. As used herein, "surface particle density" includes not only surface particles but also light-scattering defects, and crystal-originated pits (COPs), and other defects incorporated into strained layer 18. Further, strained layer 18 produced in accordance with the present invention may have a localized light-scattering defect level of less than about 0.3 defects/cm^2 for particle defects having a size (diameter) greater than 0.13 microns, a defect level of about 0.2 defects/cm^2 for particle defects having a size greater than 0.16 microns, a defect level of about 0.1 defects/cm^2 for particle defects having a size greater than 0.2 microns, and a defect level of about 0.03 defects/cm^2 for defects having a size greater than 1 micron. Process optimization may enable reduction of the localized light-scattering defect levels to about 0.09 defects/cm^2 for particle defects having a size greater than 0.09 microns and to 0.05 defects/cm^2 for particle defects having a size greater than 0.12 microns. These surface particles may be incorporated in strained layer 18 during the formation of strained layer 18, or they may result from the propagation of surface defects from an underlying layer, such as relaxed layer 16.

In alternative embodiments, graded layer 14 may be absent from the structure. Relaxed layer 16 may be formed in various ways, and the invention is not limited to embodiments having graded layer 14. In other embodiments, strained layer 18 may be formed directly on substrate 12. In this case, the strain in layer 18 may be induced by lattice mismatch between layer 18 and substrate 12, induced mechanically, e.g., by the deposition of overlayers, such as Si_3N_4, or induced by thermal mismatch between layer 18 and a subsequently grown layer, such as a SiGe layer. In some embodiments, a uniform semiconductor layer (not shown), having a thickness of

approximately 0.5 μm and comprising the same semiconductor material as substrate 12, is disposed between graded buffer layer 14 and substrate 12. This uniform semiconductor layer may be grown to improve the material quality of layers subsequently grown on substrate 12, such as graded buffer layer 14, by providing a clean, contaminant-free surface for epitaxial growth. In certain embodiments, relaxed layer 16 may be planarized prior to growth of strained layer 18 to eliminate the crosshatched surface roughness induced by graded buffer layer 14. (See, e.g., M.T. Currie, et al., *Appl. Phys. Lett.*, 72 (14) p. 1718 (1998), incorporated herein by reference.) The planarization may be performed by a method such as chemical mechanical polishing (CMP), and may improve the quality of a subsequent bonding process (see below) because it minimizes the wafer surface roughness and increases wafer flatness, thus providing a greater surface area for bonding.

Referring to Figure 1B, after planarization of relaxed layer 16, a relaxed semiconductor regrowth layer 19 including a semiconductor such as SiGe may be grown on relaxed layer 16, thus improving the quality of subsequent strained layer 18 growth by ensuring a clean surface for the growth of strained layer 18. Growing on this clean surface may be preferable to growing strained material, e.g., silicon, on a surface that is possibly contaminated by oxygen and carbon from the planarization process. The conditions for epitaxy of the relaxed semiconductor regrowth layer 19 on the planarized relaxed layer 16 should be chosen such that surface roughness of the resulting structure, including layers formed over regrowth layer 19, is minimized to ensure a surface suitable for subsequent high quality bonding. High quality bonding may be defined as the existence of a bond between two wafers that is substantially free of bubbles or voids at the interface. Measures that may help ensure a smooth surface for strained layer 18 growth, thereby facilitating bonding, include substantially matching a lattice of the semiconductor regrowth layer 19 to that of the underlying relaxed layer 16, by keeping the regrowth thickness below approximately 1 μm, and/or by keeping the growth temperature below approximately 850 °C for at least a portion of the semiconductor layer 19 growth. It may also be advantageous for relaxed layer 16 to be substantially free of particles or areas with high threading dislocation densities (i.e., threading dislocation pile-ups) which could induce non-planarity in the regrowth and decrease the quality of the subsequent bond.

Referring to Figure 2A, in an embodiment, hydrogen ions are implanted into relaxed layer 16 to define a cleave plane 20. This implantation is similar to the SMARTCUT process that has been demonstrated in silicon by, e.g., SOITEC, based in Grenoble, France. Implantation

parameters may include implantation of hydrogen (H_2^+) to a dose of 2.5- 5 x 10^{16} ions/cm^2 at an energy of, e.g., 50 - 100 keV. For example, H_2^+ may be implanted at an energy of 75 keV and a dose of 4 x 10^{16} ions/cm^2 through strained layer 18 into relaxed layer 16. In alternative embodiments, it may be favorable to implant at energies less than 50 keV to decrease the depth of cleave plane 20 and decrease the amount of material subsequently removed during the cleaving process (see discussion below with reference to Figure 4). In an alternative embodiment, other implanted species may be used, such as H^+ or He^+, with the dose and energy being adjusted accordingly. The implantation may also be performed prior to the formation of strained layer 18. Then, the subsequent growth of strained layer 18 is preferably performed at a temperature low enough to prevent premature cleaving along cleave plane 20, i.e., prior to the wafer bonding process. This cleaving temperature is a complex function of the implanted species, implanted dose, and implanted material. Typically, premature cleaving may be avoided by maintaining a growth temperature below approximately 500 °C.

In some embodiments, such as when strained layer 18 comprises nearly 100% Ge, a thin layer 21 of another material, such as Si, may be formed over strained layer 18 prior to bonding (see discussion with respect to Figure 3). This thin layer 21 may be formed to enhance subsequent bonding of strained layer 18 to an insulator, such as an oxide. Thin layer 21 may have a thickness T_{21} of, for example, 0.5 – 5 nm.

In some embodiments, strained layer 18 may be planarized by, e.g., CMP, to improve the quality of the subsequent bond. Strained layer 18 may have a low surface roughness, e.g., less than 0.5 nm root mean square (RMS). Referring to Figure 2B, in some embodiments, a dielectric layer 22 may be formed over strained layer 18 prior to ion implantation into relaxed layer 16 to improve the quality of the subsequent bond. Dielectric layer 22 may be, e.g., silicon dioxide (SiO_2) deposited by, for example, LPCVD or by high density plasma (HDP). An LPCVD deposited SiO_2 layer may be subjected to a densification step at elevated temperature. Suitable conditions for this densification step may be, for example, a 10 minute anneal at 800 °C in a nitrogen ambient. Alternatively, dielectric layer 22 may include low-temperature oxide (LTO), which may be subsequently densified at elevated temperature in nitrogen or oxygen ambients. Suitable conditions for this densification step can be a 10 minute anneal at 800 °C in an oxygen ambient. Dielectric layer 22 may be planarized by, e.g., CMP to improve the quality of the subsequent bond. In an alternative embodiment, it may be advantageous for dielectric layer 22 to be formed from thermally grown SiO_2 in order to provide a high quality

semiconductor/dielectric interface in the final structure. In an embodiment, strained layer 18 comprises approximately 100% Ge and dielectric layer 22 comprises, for example, germanium dioxide (GeO_2); germanium oxynitride (GeON); a high-k insulator having a higher dielectric constant than that of Si such as hafnium oxide (HfO_2) or hafnium silicate (HfSiON, $HfSiO_4$); or a multilayer structure including GeO_2 and SiO_2. Ge has an oxidation behavior different from that of Si, and the deposition methods may be altered accordingly.

Referring to Figure 3, epitaxial wafer 8 is bonded to a handle wafer 50. Either handle wafer 50, epitaxial wafer 8, or both have a top dielectric layer (see, e.g., dielectric layer 22 in Figure 2B) to facilitate the bonding process and to serve as an insulator layer in the final substrate structure. Handle wafer 50 may have a dielectric layer 52 disposed over a semiconductor substrate 54. Dielectric layer 52 may include, for example, SiO_2. In an embodiment, dielectric layer 52 includes a material having a melting point (T_m) higher than a T_m of pure SiO_2, i.e., higher than 1700 °C. Examples of such materials are silicon nitride (Si_3N_4), aluminum oxide, magnesium oxide, etc. Using dielectric layer 52 with a high T_m helps prevents possible relaxation of the transferred strained semiconductor layer 18 that may occur during subsequent processing, due to softening of the underlying dielectric layer 52 at temperatures typically used during device fabrication (approximately 1000 - 1200 °C). In other embodiments, handle wafer 50 may include a combination of a bulk semiconductor material and a dielectric layer, such as a silicon on insulator substrate. Semiconductor substrate 54 includes a semiconductor material such as, for example, Si, Ge, or SiGe.

Handle wafer 50 and epitaxial wafer 8 are cleaned by a wet chemical cleaning procedure to facilitate bonding, such as by a hydrophilic surface preparation process to assist the bonding of a semiconductor material, e.g., strained layer 18, to a dielectric material, e.g., dielectric layer 52. For example, a suitable prebonding surface preparation cleaning procedure could include a modified megasonic RCA SC1 clean containing ammonium hydroxide, hydrogen peroxide, and water ($NH_4OH:H_2O_2:H_2O$) at a ratio of 1:4:20 at 60 °C for 10 minutes, followed by a deionized (DI) water rinse and spin dry. The wafer bonding energy should be strong enough to sustain the subsequent layer transfer (see Figure 4). In some embodiments, top surfaces 60, 62 of handle wafer 50 and epitaxial wafer 8, including a top surface 63 of strained semiconductor layer 18, may be subjected to a plasma activation, either before, after, or instead of a wet clean, to increase the bond strength. The plasma environment may include at least one of the following species: oxygen, ammonia, argon, nitrogen, diborane, and phosphine. After an appropriate cleaning step,

handle wafer 50 and epitaxial wafer 8 are bonded together by bringing top surfaces 60, 62 in contact with each other at room temperature. The bond strength may be greater than 1000 mJ/m^2, achieved at a low temperature, such as less than 600 °C.

Referring to Figure 4 as well as to Figure 3, a split is induced at cleave plane 20 by annealing handle wafer 50 and epitaxial wafer 8 after they are bonded together. This split may be induced by an anneal at 300 - 700 °C, e.g., 550 °C, inducing hydrogen exfoliation layer transfer (i.e., along cleave plane 20) and resulting in the formation of two separate wafers 70, 72. One of these wafers (70) has a first portion 80 of relaxed layer 16 (see Figure 1A) disposed over strained layer 18. Strained layer 18 is in contact with dielectric layer 52 on semiconductor substrate 54. The other of these wafers (72) includes substrate 12, graded layer 14, and a remaining portion 82 of relaxed layer 16. In some embodiments, wafer splitting may be induced by mechanical force in addition to or instead of annealing. If necessary, wafer 70 with strained layer 18 may be annealed further at 600 - 900 °C, e.g., at a temperature greater than 800 °C, to strengthen the bond between the strained layer 18 and dielectric layer 52. In some embodiments, this anneal is limited to an upper temperature of about 900 °C to avoid the destruction of a strained Si/relaxed SiGe heterojunction by diffusion. Wafer 72 may be planarized, and used as starting substrate 8 for growth of another strained layer 18. In this manner, wafer 72 may be "recycled" and the process illustrated in Figures 1A - 5 may be repeated. An alternative "recyling" method may include providing relaxed layer 16 that is several microns thick and repeating the process illustrated in Figures 1A - 5, starting with the formation of strained layer 18. Because the formation of this thick relaxed layer 16 may lead to bowing of substrate 12, a layer including, e.g., oxide or nitride, may be formed on the backside of substrate 12 to counteract the bowing. Alternatively substrate 12 may be pre-bowed when cut and polished, in anticipation of the bow being removed by the formation of thick relaxed layer 16.

Referring to Figure 4 as well as to Figure 5, relaxed layer portion 80 is removed from strained layer 18. In an embodiment, removal of relaxed layer portion 80, containing, e.g., SiGe, includes oxidizing the relaxed layer portion 80 by wet (steam) oxidation. For example, at temperatures below approximately 800 °C, such as temperatures between 600 - 750 °C, wet oxidation will oxidize SiGe much more rapidly then Si, such that the oxidation front will effectively stop when it reaches the strained layer 18, in embodiments in which strained layer 18 includes Si. The difference between wet oxidation rates of SiGe and Si may be even greater at lower temperatures, such as approximately 400 °C - 600 °C. Good oxidation selectivity is

provided by this difference in oxidation rates, i.e., SiGe may be efficiently removed at low temperatures with oxidation stopping when strained layer 18 is reached. This wet oxidation results in the transformation of SiGe to a thermal insulator 90, e.g., $Si_xGe_yO_z$. The thermal insulator 90 resulting from this oxidation is removed in a selective wet or dry etch, e.g., wet hydrofluoric acid. In some embodiments, it may be more economical to oxidize and strip several times, instead of just once.

In certain embodiments, wet oxidation may not completely remove the relaxed layer portion 80. Here, a localized rejection of Ge may occur during oxidation, resulting in the presence of a residual Ge-rich SiGe region at the oxidation front, on the order of, for example, several nanometers in lateral extent. A surface clean may be performed to remove this residual Ge. For example, the residual Ge may be removed by a dry oxidation at, e.g., 600 °C, after the wet oxidation and strip described above. Another wet clean may be performed in conjunction with – or instead of – the dry oxidation. Examples of possible wet etches for removing residual Ge include a Piranha etch, i.e., a wet etch that is a mixture of sulfuric acid and hydrogen peroxide (H_2SO_4:H_2O_2) at a ratio of, for example, 3:1. An HF dip may be performed after the Piranha etch. Alternatively, an RCA SC1 clean may be used to remove the residual Ge. The process of Piranha or RCA SC1 etching and HF removal of resulting oxide may be repeated more than once. In an embodiment, relaxed layer portion including, e.g., SiGe, is removed by etching and annealing under a hydrochloric acid (HCl) ambient.

In the case of a strained Si layer, the surface Ge concentration of the final strained Si surface is preferably less than about $1x10^{12}$ atoms/cm^2 when measured by a technique such as total reflection x-ray fluorescence (TXRF) or the combination of vapor phase decomposition (VPD) with a spectroscopy technique such as graphite furnace atomic absorption spectroscopy (GFAAS) or inductively-coupled plasma mass spectroscopy (ICP-MS). In some embodiments, after cleaving, a planarization step or a wet oxidation step may be performed to remove a portion of the damaged relaxed layer portion 80 as well as to increase the smoothness of its surface. A smoother surface may improve the uniformity of subsequent complete removal of a remainder of relaxed layer portion 80 by, e.g., wet chemical etching. After removal of relaxed layer portion 80, strained layer 18 may be planarized. Planarization of strained layer 18 may be performed by, e.g., CMP; an anneal at a temperature greater than, for example, 800 °C, in a hydrogen (H_2) or hydrochloric acid (HCl) containing ambient; or cluster ion beam smoothing.

Referring to Figure 6, a SSOI substrate 100 has strained layer 18 disposed over an insulator, such as dielectric layer 52 formed on semiconductor substrate 54. Strained layer 18 has a thickness T_4 selected from a range of, for example, 50 - 1000 Å, with a thickness uniformity of better than approximately ±5% and a surface roughness of less than approximately 20 Å. Dielectric layer 52 has a thickness T_{52} selected from a range of, for example, 500 - 3000 Å. In an embodiment, strained layer 18 includes approximately 100% Si or 100% Ge having one or more of the following material characteristics: misfit dislocation density of, e.g., 0 - 10^5 cm/cm^2; a threading dislocation density of about 10^1-10^7 dislocations/cm^2; a surface roughness of approximately 0.01 - 1 nm RMS; and a thickness uniformity across SSOI substrate 100 of better than approximately ±10% of a mean desired thickness; and a thickness T_4 of less than approximately 200 Å. In an embodiment, SSOI substrate 100 has a thickness uniformity of better than approximately ±5% of a mean desired thickness.

In an embodiment, dielectric layer 52 has a T_m greater than that of SiO_2. During subsequent processing, e.g., MOSFET formation, SSOI substrate 100 may be subjected to high temperatures, i.e., up to 1100 °C. High temperatures may result in the relaxation of strained layer 18 at an interface between strained layer 18 and dielectric layer 52. The use of dielectric layer with a T_m greater than 1700 °C may help keep strained layer 18 from relaxing at the interface between strained layer 18 and dielectric layer 52 when SSOI substrate is subjected to high temperatures.

In an embodiment, the misfit dislocation density of strained layer 18 may be lower than its initial dislocation density. The initial dislocation density may be lowered by, for example, performing an etch of a top surface 92 of strained layer 18. This etch may be a wet etch, such as a standard microelectronics clean step such as an RCA SC1, i.e., hydrogen peroxide, ammonium hydroxide, and water ($H_2O_2 + NH_4OH + H_2O$), which at, e.g., 80 °C may remove silicon.

The presence of surface particles on strained layer 18, as described above with reference to Figure 1A, may result in the formation of bonding voids at an interface 102 between strained layer 18 and dielectric layer 52. These bonding voids may have a density equivalent to the density of surface particles formed on strained layer 18, e.g., less than about 0.3 voids/cm^2.

In some embodiments, strained semiconductor layer 18 includes Si and is substantially free of Ge; further, any other layer disposed in contact with strained semiconductor layer 18 prior to device processing, e.g., dielectric layer 52, is also substantially free of Ge.

Referring to Figure 7, in an alternative embodiment, relaxed layer portion 80 may be removed by a selective wet etch that stops at the strained layer 18 to obtain SSOI substrate 100 (see Fig. 6). In embodiments in which relaxed layer portion 80 contains SiGe, a suitable selective SiGe wet etch may be a solution containing nitric acid (HNO_3) and dilute HF at a ratio of 3:1 or a solution containing H_2O_2, HF, and acetic acid (CH_3COOH) at a ratio of 2:1:3. Alternatively, relaxed layer portion 80 may be removed by a dry etch that stops at strained layer 18. In some embodiments, relaxed layer portion 80 may be removed completely or in part by a chemical-mechanical polishing step or by mechanical grinding.

Strained semiconductor-on-insulator substrate 100 may be further processed by CMOS SOI MOSFET fabrication methods. For example, referring to Figure 8A, a transistor 200 may be formed on SSOI substrate 100. Forming transistor 200 includes forming a gate dielectric layer 210 above strained layer 18 by, for example, growing an SiO_2 layer by thermal oxidation. Alternatively, gate dielectric layer 210 may include a high-k material with a dielectric constant higher than that of SiO_2, such as HfO_2, HfSiON, or $HfSiO_4$. In some embodiments, gate dielectric layer 210 may be a stacked structure, e.g., a thin SiO_2 layer capped with a high-k material. A gate 212 is formed over gate dielectric layer 210. Gate 212 may be formed of a conductive material, such as doped semiconductor, e.g., polycrystalline Si or polycrystalline SiGe; a metal, e.g., titanium (Ti), tungsten (W), molybdenum (Mo), tantalum (Ta), nickel (Ni), or iridium (Ir); or metal compounds, e.g., titanium nitride (TiN), titanium silicon nitride (TiSiN), tungsten nitride (WN), tantalum nitride (TaN), tantalum silicide (TaSi), nickel silicide (NiSi), or iridium oxide (IrO_2), that provide an appropriate workfunction. A source region 214 and a drain region 216 are formed in a portion 218 of strained semiconductor layer 18, proximate gate dielectric layer 210. Source and drain regions 214, 216 may be formed by, e.g., ion implantation of either n-type or p-type dopants.

In some embodiments, strained semiconductor layer 18 may be compressively strained when, for example, layer 18 includes strained Ge. Compressively strained layers may be prone to undulation when subjected to large temperature changes. The risk of such undulation may be reduced by reducing the thermal budget of a process for fabricating devices, such as transistor 200. The thermal budget may reduced by, for example, using atomic layer deposition (ALD) to deposit gate dielectric layer 210. Furthermore, a maximum temperature for forming gate 212 may be limited to, e.g., 600 °C by, for example, the use of materials comprising metal or metal

compounds, rather than polysilicon or other gate materials that may require higher formation and/or dopant activation temperatures.

Referring to Figure 8B, a transistor 250 formed on SSOI substrate 100 may have an elevated source region and an elevated drain region proximate a first and a second sidewall spacer 252, 254. These elevated regions may be formed as follows. A semiconductor layer 256a –256c is formed selectively on exposed silicon surfaces, i.e., on top surface 258 of a gate 259 containing silicon, a top surface 260 of a source 262 defined in strained layer 18, and top surface 264 of a drain 266 defined in strained layer 18. In an embodiment, semiconductor layer 256a – 256c is an epitaxial layer, such as epitaxial silicon, epitaxial germanium, or epitaxial silicon-germanium. No semiconductor layer is formed on non-silicon features, such as sidewall spacers 252, 254 and dielectric isolation regions 268, 270. Semiconductor layer 256a – 256c has a thickness T_{256} of, for example, approximately 100 – 500 Å.

Semiconductor layer 256a – 256c has a low resistivity of, e.g., 0.001 ohm-cm, that facilitates the formation of low-resistance contacts. To achieve this low resistivity, semiconductor layer 256a – 256c is, for example, epitaxial silicon doped with, for example, arsenic to a concentration of 1×10^{20} atoms/cm^3. Semiconductor layer 256a – 256c may be doped in situ, during deposition. In alternative embodiments, semiconductor layer 256a – 256c may be doped after deposition by ion implantation or by gas-, plasma- or solid-source diffusion. In some embodiments, the doping of semiconductor layer 256a – 256c and the formation of source 262 and drain 266 are performed simultaneously. Portions of semiconductor layer 256a, 256c disposed over source 262 and drain 266 may have top surfaces substantially free of facets. In an embodiment, portions of source 262, drain 266, and/or gate 259 may be etched away to define recess prior to deposition of semiconductor layer 256a – 256c, and semiconductor layer 256a – 256c may then be deposited in the recesses thus formed.

Referring to Figure 8C, a metal layer 272 is formed over transistor 250. Metal layer 272 is formed by, for example, sputter deposition. Metal layer 272 has a thickness T_{272} of, e.g., 50 - 200 Å and includes a metal such as cobalt, titanium, tungsten, nickel, or platinum. The metal is selected to react with semiconductor layer 256a – 256c to form a low-resistance metal-semiconductor alloy when exposed to heat, as described below. The metal is also selected such that the metal-semiconductor alloy remains stable at temperatures typically required to complete transistor 250 fabrication, e.g., 400 - 700°C.

Referring also to Figure 8D, subsequent to deposition of metal layer 272, a first rapid thermal anneal is performed, e.g., at 550°C for 60 seconds. This heating step initiates a reaction between metal layer 272 and semiconductor layers 256a – 256c, forming a high resistivity phase of a metal-semiconductor alloy, e.g., cobalt silicide (CoSi). Portions of metal layer 272 are removed by a wet etch, such as sulfuric acid and hydrogen peroxide. In an alternative embodiment, the wet etch may be ammonium hydroxide, peroxide, and water. This wet etch removes portions of metal layer 272 disposed over dielectric material, such as over first and second sidewall spacers 252, 254 and isolation regions 268, 270. Portions 274 of metal layer 272 disposed over semiconductor layer 256a – 256c that have reacted to form the metal-semiconductor alloy remain in place after the anneal and wet etch.

Referring to Figure 8E, SSOI substrate 100, including transistor 250, is subjected to a second heat treatment. For example, in an embodiment in which metal layer 272 includes cobalt, SSOI substrate 100 undergoes a rapid thermal anneal at 800°C for 60 seconds in a nitrogen ambient. This heating step initiates a reaction in the metal-semiconductor alloy layer which substantially lowers its resistivity, to form a substantially homogeneous contact layer 276a – 276c. Contact layer 276a – 276c includes a metal-semiconductor alloy, e.g., a metal silicide such as a low resistivity phase of cobalt silicide ($CoSi_2$). Contact layer 276a – 276c has a thickness T_{276} of, for example, 400 Å. Contact layer 276a – 276c has a low sheet resistance, e.g., less than about 10 Ω/□, and enables a good quality contact to be made to source 262 and drain 266, as well as to gate 259.

In some embodiments, during formation, contact layer 276a – 276c may consume substantially all of semiconductor layer 256a – 256c. A bottommost boundary 278a of contact layer 276a, therefore, shares an interface 280a with strained layer 18 in source 262, and a bottommost boundary 278c of contact layer 276c, therefore, shares an interface 280c with strained layer 18 in drain 266. A bottommost boundary 278b of contact layer 276b shares an interface 280b with gate 259.

In other embodiments, contact layer portions 276a, 276c, disposed over source 262 and drain 266, may extend into strained layer 18. Interfaces 280a, 280c between contact layer 276a, 276c and strained layer 18 are then disposed within source 262 and drain 266, respectively, above bottommost boundaries 282a, 282c of strained layer 18. Interfaces 280a, 280c have a low contact resistivity, e.g., less than approximately 5×10^{-7} Ω-cm^2. In certain other embodiments, during formation, contact layer 276a – 276c may not consume all of semiconductor layer 256a –

256c (see Figure 8D). A bottommost boundary 278a of contact layer 276a, therefore, shares an interface with semiconductor layer 256a over source 262, and a bottommost boundary 278c of contact layer 276c, therefore, shares an interface with semiconductor layer 256c over drain 266.

Because strained layer 18 includes a strained material, carrier mobilities in strained layer 18 are enhanced, facilitating lower sheet resistances. This strain also results in a reduced energy bandgap, thereby lowering the contact resistivity between the metal-semiconductor alloy and the strained layer.

In alternative embodiments, an SSOI structure may include, instead of a single strained layer, a plurality of semiconductor layers disposed on an insulator layer. For example, referring to Figure 9, epitaxial wafer 300 includes strained layer 18, relaxed layer 16, graded layer 14, and substrate 12. In addition, a semiconductor layer 310 is disposed over strained layer 18. Strained layer 18 may be tensilely strained and semiconductor layer 310 may be compressively strained. In an alternative embodiment, strained layer 18 may be compressively strained and semiconductor layer 310 may be tensilely strained. Strain may be induced by lattice mismatch with respect to an adjacent layer, as described above, or mechanically. For example, strain may be induced by the deposition of overlayers, such as Si_3N_4. In another embodiment, semiconductor layer 310 is relaxed. Semiconductor layer 310 includes a semiconductor material, such as at least one of a group II, a group III, a group IV, a group V, and a group VI element. Epitaxial wafer 300 is processed in a manner analogous to the processing of epitaxial wafer 8, as described with reference to Figures 1 - 7.

Referring also to Figure 10, processing of epitaxial wafer 300 results in the formation of SSOI substrate 350, having strained layer 18 disposed over semiconductor layer 310. Semiconductor layer 310 is bonded to dielectric layer 52, disposed over substrate 54. As noted above with reference to Figure 9, strained layer 18 may be tensilely strained and semiconductor layer 310 may be compressively strained. Alternatively, strained layer 18 may be compressively strained and semiconductor layer 310 may be tensilely strained. In some embodiments, semiconductor layer 310 may be relaxed.

Referring to Figure 11, in some embodiments, a thin strained layer 84 may be grown between strained layer 18 and relaxed layer 16 to act as an etch stop during etching, such as wet etching. In an embodiment in which strained layer 18 includes Si and relaxed layer 16 includes $Si_{1-y}Ge_y$, thin strained layer 84 may include $Si_{1-x}Ge_x$, with a higher Ge content (x) than the Ge content (y) of relaxed layer 16, and hence be compressively strained. For example, if the

composition of the relaxed layer 16 is 20% Ge ($Si_{0.80}Ge_{0.20}$), thin strained layer 84 may contain 40% Ge ($Si_{0.60}Ge_{0.40}$) to provide a more robust etch stop. In other embodiments, a second strained layer, such as thin strained layer 84 with higher Ge content than relaxed layer 16, may act as a preferential cleave plane in the hydrogen exfoliation/cleaving procedure described above.

In an alternative embodiment, thin strained layer 84 may contain $Si_{1-x}Ge_x$ with lower Ge content than relaxed layer 16. In this embodiment, thin strained layer 84 may act as a diffusion barrier during the wet oxidation process. For example, if the composition of relaxed layer 16 is 20% Ge ($Si_{0.80}Ge_{0.20}$), thin strained layer 84 may contain 10% Ge ($Si_{0.90}Ge_{0.10}$) to provide a barrier to Ge diffusion from the higher Ge content relaxed layer 16 during the oxidation process. In another embodiment, thin strained layer 84 may be replaced with a thin graded $Si_{1-z}Ge_z$ layer in which the Ge composition (z) of the graded layer is decreased from relaxed layer 16 to the strained layer 18.

Referring again to Figure 7, in some embodiments, a small amount, e.g., approximately 20 - 100 Å, of strained layer 18 may be removed at an interface 105 between strained layer 18 and relaxed layer portion 80. This may be achieved by overetching after relaxed layer portion 80 is removed. Alternatively, this removal of strained layer 18 may be performed by a standard microelectronics clean step such as an RCA SC1, i.e., hydrogen peroxide, ammonium hydroxide, and water ($H_2O_2 + NH_4OH + H_2O$), which at, e.g., 80°C may remove silicon. This silicon removal may remove any misfit dislocations that formed at the original strained layer 18/relaxed layer 80 interface 105 if strained layer 18 was grown above the critical thickness. The critical thickness may be defined as the thickness of strained layer 18 beyond which it becomes energetically favorable for the strain in the layer to partially relax via the introduction of misfit dislocations at interface 105 between strained layer 18 and relaxed layer 16. Thus, the method illustrated in Figures 1 - 7 provides a technique for obtaining strained layers above a critical thickness without misfit dislocations that may compromise the performance of deeply scaled MOSFET devices.

Referring to Figure 12, in some embodiments, handle wafer 50 may have a structure other than a dielectric layer 52 disposed over a semiconductor substrate 54. For example, a bulk relaxed substrate 400 may comprise a bulk material 410 such as a semiconductor material, e.g., bulk silicon. Alternatively, bulk material 410 may be a bulk dielectric material, such as Al_2O_3 (e.g., alumina or sapphire) or SiO_2 (e.g., quartz). Epitaxial wafer 8 may then be bonded to

handle wafer 400 (as described above with reference to Figures 1 - 6), with strained layer 18 being bonded to the bulk material 410 comprising handle wafer 400. In embodiments in which bulk material 410 is a semiconductor, to facilitate this semiconductor-semiconductor bond, a hydrophobic clean may be performed, such as an HF dip after an RCA SC1 clean.

Referring to Figure 13, after bonding and further processing (as described above), a strained-semiconductor-on-semiconductor (SSOS) substrate 420 is formed, having strained layer 18 disposed in contact with relaxed substrate 400. The strain of strained layer 18 is not induced by underlying relaxed substrate 400, and is independent of any lattice mismatch between strained layer 18 and relaxed substrate 400. In an embodiment, strained layer 18 and relaxed substrate 400 include the same semiconductor material, e.g., silicon. Relaxed substrate 400 may have a lattice constant equal to a lattice constant of strained layer 18 in the absence of strain. Strained layer 18 may have a strain greater than approximately 1×10^{-3}. Strained layer 18 may have been formed by epitaxy, and may have a thickness T_5 of between approximately 20 Å - 1000 Å, with a thickness uniformity of better than approximately ±10%. In an embodiment, strained layer 18 may have a thickness uniformity of better than approximately ±5%. Surface 92 of strained layer 18 may have a surface roughness of less than 20 Å.

Referring to Figure 14, in an embodiment, after fabrication of the SSOI structure 100 including semiconductor substrate 54 and dielectric layer 52, it may be favorable to selectively relax the strain in at least a portion of strained layer 18. This could be accomplished by introducing a plurality of ions by, e.g., ion implantation after a photolithography step in which at least a portion of the structure is masked by, for example, a photoresist feature 500. Ion implantation parameters may be, for example, an implant of Si ions at a dose of 1×10^{15} - 1×10^{17} ions/cm^2, at an energy of 5 - 75 keV. After ion implantation, a relaxed portion 502 of strained layer 18 is relaxed, while a strained portion 504 of strained layer 18 remains strained.

DEVICES

In addition to the transistors described above with reference to Figures 8A - 8E, various other transistors may be formed on SSOI substrate 100 fabricated by the methods described above All of these transistors may also be formed on SSOI substrate 100 fabricated with the use of a porous semiconductor substrate, as described below with reference to Figures 40A - 41D.

finFET

A finFET (or any variant of the basic finFET structure such as the wrap-around gate FET, tri-gate FET, or omega FET) may be fabricated on SSOI substrate 100 as described below. The

finFET and related devices include two gates located on either side of a FET channel region. Unlike in a traditional planar FET, this channel region is raised above the wafer surface: the channel (or portions of the channel) falls in a plane perpendicular to the wafer surface. There may in addition be gates above and/or below the channel region, such as in the wrap-around gate FET.

Referring to Figure 15, SSOI substrate 100 includes strained layer 18 and dielectric layer 52 disposed over substrate 54. In an embodiment, strained layer 18 includes Si and has thickness T_6 of, e.g., 200 - 1000 Å. Dielectric layer 52 may be formed from SiO_2, with thickness T_7 selected from the range of, e.g., 500 - 3000 Å. Substrate 54 may be formed from, e.g., Si.

Referring to Figures 16A and 16B, strained layer 18 is patterned to define a plurality of fins 600. Fins 600 are defined by the formation of a photolithographic mask (not shown) over strained layer 18, followed by anisotropic reactive ion etching (RIE) of strained layer 18. Fins 600 have a width W_1 of, e.g., 50 - 300 Å. The photomask/RIE steps also define source mesa region 602 and drain mesa region 604. Fins 600, source mesa region 602, and source mesa region 604 include portions of strained layer 18 not removed by RIE. The photolithographic mask is removed after the RIE of strained layer 18.

Referring to Figure 17, a gate insulator layer 610 is formed over SSOI substrate 100. Gate insulator layer 610 is conformally formed over fins 600, as well as over source and drain mesa regions 602, 604. Gate insulator layer 610 may include, e.g., thermally grown SiO_2, or a high-k dielectric like HfO_2 or HfSiON, and have a thickness T_8 of, e.g., 10 - 100 Å. In some embodiments, gate insulator layer 610 is grown, and is therefore formed only over exposed silicon surfaces, i.e., over fins 600 and source and drain mesa regions 602, 604. In other embodiments, gate insulator layer 610 is deposited, and is therefore formed over an entire top surface of SSOI substrate 100.

Referring to Figures 18A and 18B, a gate electrode material 620 is conformally formed over gate insulator layer 610, including over fins 600. Gate electrode material 620 may be, e.g., polycrystalline silicon ("polysilicon"), deposited by CVD, such as by UHVCVD, APCVD, LPCVD, or PECVD, having a thickness T_{62} selected from the range of, e.g., 100 - 2000 Å. A photolithographic mask (not shown) is formed over gate electrode material 620. Portions of gate electrode material 620 are selectively removed by, e.g., RIE to define a gate 622 crossing over fins 600, and terminating in a gate contact area 624. Portions of gate insulator layer 610 are exposed (or even removed) by the RIE of gate electrode material 620.

Referring to Figures 19A and 19B, a plurality of dopants are introduced into source and drain mesa regions 602, 604 to define source 630 and drain 632. To form an n-type finFET, dopants such as arsenic or phosphorus may be implanted into mesa regions 602, 604. Possible implantation parameters may be, for example, arsenic with a dose of 2×10^{15} atoms/cm^2 implanted at an energy of 10 - 50 kilo-electron volts (keV). To form a p-type finFET, dopants such as boron may be implanted into mesa regions 602, 604. Possible implantation parameters may be, for example, boron, with a dose of 2×10^{15} atoms/cm^2 at an energy of 3 - 15 keV. For the formation of a CMOS device, NMOS regions may be protected by a mask during the implantation of p-type dopants into PMOS regions. Similarly, PMOS regions may be protected by a mask during the implantation of n-type dopants into NMOS regions. A suitable mask for both types of implantation may be, e.g., photoresist.

During the introduction of dopants into source and drain mesa regions 602, 604, a plurality of gate dopants 634 are also introduced into gate 622 and gate contact area 624. Gate dopants 634 serve to increase a conductivity of gate electrode material 620. Gate dopants 630 may be, for example, implanted arsenic or phosphorous ions for an n-type finFET.

Dopants for both n-type and p-type finFETs may be implanted at an angle of 20 - 50°, with zero degrees being normal to SSOI substrate 100. Implanting at an angle may be desired in order to implant ions into a side of exposed fins 600 and also into a side of the vertical surfaces of gate electrode material 620.

Referring to Figures 20A and 20B, a blanket layer of spacer insulator material is formed over SSOI substrate 100, including over gate 622, gate contact 624, source 630, and drain 632. Spacer insulator material may be, for example, SiO_2 or Si_3N_4 deposited by CVD and have a thickness T_9 of, for example, 100 - 1000 Å. Subsequently, portions of spacer insulator material are removed by an anisotropic RIE to define a plurality of sidewall spacers 642 proximate vertical surfaces, such as fins 600, gate 622, and gate contact area 624. Horizontal surfaces, such as top surfaces of fins 600, are substantially free of the spacer insulator material.

After the RIE definition of sidewall spacers 642, the portions of gate insulator layer 610 exposed by the RIE of gate electrode material 620 may be removed from top surfaces of source 630, and drain 632 by, e.g., a dip in hydrofluoric acid (HF), such as for 5 - 30 seconds in a solution containing, e.g., 0.5 - 5% HF. Alternately, this removal may be via RIE, with an etchant species such as, e.g., CHF_3.

Referring to Figures 21A and 21B, a self-aligned silicide ("salicide") is formed over SSOI substrate 100 to provide low resistance contacts as follows. A conductive layer is formed over SSOI substrate 100. For example, a metal such as cobalt or nickel is deposited by, e.g., CVD or sputtering, with the conductive layer having a thickness of, e.g., 50 - 200 Å. An anneal is performed to react the conductive layer with the underlying semiconductor, e.g., exposed portions of gate 622 and gate contact area 624, to form salicide 650 including, e.g., cobalt silicide or nickel silicide. Anneal parameters may be, for example, 400 - 800 °C for 10 - 120 seconds. Unreacted portions of the conductive layer disposed directly over insulator material, such as exposed portions of dielectric layer 52 and sidewall spacers 642, are removed by a chemical strip. A suitable chemical strip may be a solution including H_2SO_4:H_2O_2 at a ratio of 3:1. A second anneal may be performed to further lower resistivity of salicide 650. The second anneal parameters may be, for example, 600 - 900 °C for 10 - 120 seconds. A finFET 655 includes fins 600, gate insulator 610, source 630, drain 632, and gate 622. A finFET 655 having three fins 600 is illustrated in Figure 21B. The three fins 600 share a common source 630 and a common drain 632. A single transistor may have multiple fins to increase current drive in comparison to a transistor with a single fin.

In an alternative embodiment, gate dielectric material may be removed from the top surfaces of the source and drain mesa regions immediately after the RIE of the gate electrode. In some embodiments, raised source and drain regions may be formed, as described above with reference to Figures 8B-8D.

Double gate MOSFETs

Referring to Figure 22 as well as to Figure 1A, epitaxial wafer 8 has layers 10 disposed over substrate 12. Substrate 12 may be formed of a semiconductor, such as Si, Ge, or SiGe. The plurality of layers 10 includes graded buffer layer 14, formed of $Si_{1-y}Ge_y$, with a maximum Ge content of, e.g., 10 - 80% (i.e., y = 0.1 - 0.8). Relaxed layer 16 is disposed over graded buffer layer 14. Relaxed layer 16 may be formed of uniform $Si_{1-x}Ge_x$ having a Ge content of, for example, 10 - 80 % (i.e., x = 0.1 - 0.8). Strained semiconductor layer 18 is disposed over relaxed layer 16. Strained layer 18 comprises at least one of a group II, a group III, a group IV, a group V, and a group VI element. Strained layer 18 may include, for example, Si and may be tensilely strained.

A first gate insulator layer 700 is formed over strained layer 18. First gate insulator layer 700 may include SiO_2 or a high-k dielectric like HfO_2 or HfSiON, and may be grown or

deposited. First gate insulator layer 700 may have a thickness T_{11} of, e.g., 10 - 100 Å. A first gate electrode layer 702 is formed over first gate insulator layer 700. First gate electrode layer 702 may include a conductive material, for example, doped polycrystalline silicon or tungsten, and may have a thickness T_{12} of, for example, 500 - 2000 Å.

Referring to Figure 23, ions 704 are introduced to define cleave plane 20 in relaxed layer 16, in the manner described above with reference to Figure 2A.

Referring to Figure 24, epitaxial wafer 8 is bonded to handle wafer 50, in the manner described above with reference to Figure 3. Handle wafer 50 includes dielectric layer 52 disposed over semiconductor substrate 54.

Referring to Figure 25 as well as to Figure 24, the bond between epitaxial wafer 8 and handle wafer 50 may be strengthened by an anneal at a relatively low temperature such as, e.g., 200 - 300 °C. Epitaxial wafer 8 is separated from handle wafer 50 by inducing a split along cleave plane 20 with an anneal at, e.g., 300 - 700 °C. After cleaving, a SSOI substrate 710 includes strained layer 18 disposed over first gate insulator 700, first gate electrode layer 702, insulator 52, and substrate 54. Residual portion 80 of relaxed layer 16 is disposed over strained layer 18. Relaxed layer portion 80 is selectively removed by, e.g., thermal oxidation and HF strip in the manner discussed above with reference to Figures 4 and 5.

Referring to Figure 26, a second gate insulator layer 720 is formed over strained layer 18. Second gate insulator layer 720 may include SiO_2 or a high-k dielectric like HfO_2 or HfSiON, and may be grown or deposited. First gate insulator layer 720 may have a thickness T_{13} of, e.g., 10 - 100 Å. A second gate electrode layer 722 is formed over second gate insulator layer 720. Second gate electrode layer 722 may include a conductive material such as, for example, doped polycrystalline silicon, and may have a thickness T_{14} of, for example, 500 - 2000 Å.

Referring to Figure 27 as well as to Figure 26, second gate electrode layer 722 is patterned by photolithography and RIE to define a second gate electrode 730. A source 732 and a drain 734 are formed in strained layer 18 by, e.g., implanting dopants, such as n-type or p-type dopants, into strained layer 18. A spacer dielectric layer is deposited and etched back to define dielectric sidewall spacers 736 proximate second gate electrode 730.

Referring to Figure 28, a conductive spacer layer 740 is deposited over strained layer 18, second gate electrode 730, and dielectric sidewall spacers 736. Conductive spacer layer 740 includes a conductive material, such as doped polycrystalline silicon or a metal. Conductive spacer layer 740 has a thickness T_{15} of, e.g., 500 - 2000 Å.

Referring to Figure 29 as well as to Figure 28, conductive spacer layer 740 is anisotropically etched to form conductive sidewall spacers 742, proximate dielectric sidewall spacers 736.

Referring to Figure 30 as well as to Figure 29, an RIE is performed to remove portions of strained layer 18, first gate insulator layer 700, and first gate electrode layer 702 not disposed directly below second gate electrode 730, dielectric sidewall spacers 736, and conductive sidewall spacers 742. After this RIE, a vertical structure 744 includes strained layer 18, first gate insulator layer 700, and first gate electrode layer 702 regions disposed under second gate electrode 730 and sidewall spacers 736, 742. Vertical structure 744 has a width W_2 of, e.g., 1000 - 5000 Å

Referring to Figure 31, an isotropic etch is performed to laterally shrink first gate electrode layer 702 region disposed under second gate electrode 730, thus defining first gate electrode 750. This isotropic etch may be a wet etch, such as hydrogen peroxide (in an embodiment in which first gate electrode layer 702 includes tungsten) or an isotropic dry etch. The width of first gate electrode layer 702 may be reduced such that both the first gate electrode 750 and the second gate electrode 730 have approximately the same width W_3 that is less than W_2, e.g., 100 - 2000 Å.

Referring to Figure 32, a thick insulator layer 760 is deposited over insulator layer 52 and vertical structure 744, i.e., over second gate electrode 730 and conductive sidewall spacers 742, as well as proximate strained layer 18, first gate insulator layer 700, and first gate electrode 750. Thick insulator layer 760 has an initial thickness T_{16} over insulator 52 of, e.g., 5000 Å. Thick insulator layer 760 is then planarized by, e.g., CMP.

Referring to Figures 33 - 35, contact holes 770 are formed through thick insulator layer 760 to conductive sidewall spacers 742 and second gate electrode 730. Contact holes 770 may be defined by the use of photolithography and RIE. Contact holes 770 are filled with a conductive material such as, e.g., a metal such as titanium or tungsten. The conductive material is patterned by photolithography and etch to define contacts 780 to source 732, drain 734, first gate electrode 750 at a first gate electrode 793, and second gate electrode 730 at a second gate electrode 795. Double gate transistor 790 includes first gate electrode 750, second gate electrode 730, first gate insulator layer 700, second gate insulator layer 722, source 732, and drain 734.

Heterojunction bipolar transistor

Referring to Figure 36 as well as to Figure 6, a heterojunction bipolar transistor (HBT) may be formed on SSOI substrate 100, including strained layer 18, dielectric layer 52, and substrate 54. A collector 810 for the HBT is formed in a portion of strained layer 18 by the introduction of dopants into the strained layer 18 portion. Collector 810 includes a low-doped region 811 and a high-doped region 812. Low-doped region 811 is doped at a relatively low level, for example at 5×10^{16} - 1×10^{18} atoms/cm^3, and has a thickness T_{20} of, for example, 100 - 1000 Å. High-doped region 812 is doped to a level not less than the doping level of low-doped region 811, preferably to a relatively high level of, e.g., 1×10^{19} - 1×10^{21} atoms/cm^3. Low-doped region 811 and high-doped region 812 are doped with the same type of dopants, and both may be doped either n-type or p-type. In an embodiment, both regions are doped n-type. Collector 810 may be electrically isolated from other devices formed on the substrate through the use of, for example, trench isolation (not shown).

A total thickness T_{21} of collector 810 may be increased to improve performance by subsequent additional deposition of a material that is lattice matched to the original strained layer 18 portion. The additional material may be, for example, SiGe lattice-matched to strained layer 18.

Referring to Figure 37, a masking layer is formed over collector 810. The masking layer may include a dielectric material, such as, e.g., SiO_2 or Si_3N_4. Photoresist is disposed over the masking layer and patterned to expose an area of the masking layer. This area is removed by, e.g., wet etching or RIE, to define a mask 910 disposed over strained layer 18. Mask 910 exposes a region 920 of collector 810.

Referring to Figure 38, a base 1010 is formed over region 920 of collector 810. Base 1010 may be formed selectively by, e.g., selective deposition of a semiconductor material only over region 920 defined by mask 910. The selective deposition can be done by CVD methods, such as by APCVD, LPCVD, UHVCVD, or by MBE. In an embodiment, base 1010 may be deposited non-selectively. The non-selectively grown material will thus also form on a top surface 1012 of mask 910, and may be removed by further photolithography and etch steps. Base 1010 has a thickness T_{22} of, e.g., of 50 - 1000 Å. In an embodiment, T_{22} may be, for example 300 - 500 Å. Base 1010 includes a semiconductor material like Si or SiGe. In some embodiments, base 1010 is relaxed or compressively strained. The in-plane lattice constant of collector 810 (strained layer 18) was defined by relaxed layer 16 (see Figure 1A). Therefore, in order that base 1010 be relaxed, the Ge content of base 1010 should be equal to the Ge content of

relaxed layer 16 (see Figure 1A). Similarly, in order that base 1010 be compressively strained, the Ge content of base 1010 should be greater than the Ge content of relaxed layer 16. This difference in Ge content also provides a base 1010 with a bandgap no larger than that of collector 810, which can be advantageous to device operation. In other embodiments, base 1010 is tensilely strained. In order that base 1010 be tensilely strained, the Ge content of base 1010 should be less than the Ge content of relaxed layer 16 (see Figure 1A). Alternatively, base 1010 may be formed from the same material as collector 810, for example strained Si. Base 1010 is doped the opposite doping type as the collector, i.e., base 1010 is p-type doped for an n-type doped collector. Base 1010 may be doped during the deposition process, but may also be doped after deposition by ion implantation. Base 1010 may be doped to a level of 1×10^{18} - 1×10^{19} atoms/cm^3.

In some embodiments, the base doping may be significantly higher, e.g., $\geq 10^{20}$ atoms/cm^3. In such embodiments, the outdiffusion of dopants from base 1010 may be deleterious to device performance, and therefore the p-type doping of base 1010 may be reduced within base 1010 in regions adjacent to an emitter 1110/base 1010 interface (see Figure 39) and a base 1010/collector 810 interface 1014 . These regions with reduced doping may have thicknesses of, e.g., 10 Å - 30 Å.

In an embodiment, base 1010 contains an element with a concentration of 1×10^{18} - 1×10^{20} atoms/cm^3 that suppresses the diffusion of dopants out of base 1010 during subsequent high temperature processing steps. A suitable element for diffusion suppression may be, for example, carbon. In another embodiment, base 1010 may be formed of SiGe, with the Ge content of base 1010 being not uniform across the thickness of base 1010. In this case, the Ge content of base 1010 may be graded in concentration, with higher Ge content at base-collector interface 1014 and lower Ge content at a base upper surface 1016. In other embodiments, the Ge content of base 1010 can have a trapezoidal or triangular profile.

Referring to Figure 39, an emitter 1110 is formed on base 1010. Emitter 1110 may be formed by the deposition of a semiconductor layer over base 1010 and mask 910. The semiconductor layer may be subsequently patterned by photolithographic and etch steps to define emitter 1110. Emitter 1110 may include a semiconductor material such as Si or SiGe, and may have a Ge content lower than the Ge content of base 1010. In an embodiment, emitter 1110 has a Ge content equal to that of relaxed layer 16 (see Figure 1A) that originally defined the in-plane lattice constant of strained layer 18 (and hence collector 810). In another embodiment, the

Ge content of emitter 1110 may be lower than that of relaxed layer 16, and, therefore, emitter 1110 is tensilely strained. In another embodiment, emitter 1110 may include the same material as strained layer 18/collector 810, such as, for example, strained Si.

Emitter 1110 has two regions: an upper emitter region 1111 and a lower emitter region 1112. Lower emitter region 1112 has a thickness T_{23} of 10 - 2000 Å and is doped with a same doping type as collector 810 (and hence the opposite doping type of base 1010). For example, lower emitter region 1112 and collector 810 may be doped n-type and base 1010 may be doped p-type. Lower emitter region 1112 may be doped at a concentration of 1×10^{17} - 5×10^{18} atoms/cm^3, for example 1×10^{18} atoms/cm^3. Upper emitter region 1111 has a thickness T_{24} of, for example, 100 - 4000 Å and is doped the same doping type as lower emitter region 1112. Upper emitter region 1111 may be doped at a concentration of 1×10^{19} - 1×10^{21} atoms/cm^3, for example 1×10^{20} - 5×10^{20} atoms/cm^3. An HBT 1200 includes collector 810, base 1010, and emitter 1110.

After formation of emitter 1110, metal contacts (not shown) may be made to each of collector 810, base 1010, and emitter 1110. Mask 910 may be removed or further patterned during the formation of metal contacts. HBT 1200 may be a standalone device or may be interconnected to other devices fabricated on SSOI substrate 100, such as, for example, transistor 200 (see Figure 8A), finFET 655 (see Figures 21A and 21B), or double-gate transistor 790 (see Figure 33).

In an embodiment, HBT 1200 may be formed on SSOS substrate 420 (see Figure 13) by the steps described above with reference to Figures 36 - 39. In another embodiment, HBT 1200 may be formed on relaxed portion 504 of strained layer 18 (see Figure 14) by the steps described above with reference to Figures 36 - 39. In this embodiment, collector 810 is formed in relaxed portion 504.

In another embodiment, HBT 1200 may be formed on a region of SSOI substrate 100 (see Figure 6) in which portions of strained layer 18 and dielectric layer 52 have been removed by the steps described with reference to Figures 36 - 39. In this embodiment, collector 810 is formed in substrate 54 and may be increased in thickness by deposition of another semiconductor layer as described above. This configuration enables the interconnection of HBT 1200 formed directly on semiconductor substrate 54 with devices formed on other portions of SSOI substrate 100, for example transistor 200 of Figure 8A.

Formation of SSOI substrate by use of a porous semiconductor substrate

Referring to Figures 40A - 40E, SSOI structure 100 (see Figure 6) may be formed by the use of a porous semiconductor substrate. Referring to Figure 40A, substrate 12 may be formed of a semiconductor, such as Si, Ge, or SiGe. A plurality of pores 1514, i.e., microvoids, are formed to define a porous layer 1516 in a portion of substrate 12. Pores 1514 may have a median diameter of 5 - 10 nm and a pitch of 10 - 50 nm. Porous layer 1516 may have a porosity of 10 - 50% and may extend a depth of d_{15} into substrate 12 of approximately 1 - 5 μm.

Referring to Figure 40B, pores 1514 may be formed by, for example, submerging substrate 12 into a vessel 1517 containing an electrolyte 1518, such as hydrofluoric acid (HF), possibly mixed with ethanol, with a cathode 1520 and an anode 1522 disposed in the electrolyte 1518. A back surface chucking holder 1519a with a vacuum pad 1519b may hold substrate 12 while it is submerged in vessel 1517. A current may be generated between cathode 1520 and anode 1522, through substrate 12, resulting in the electrochemical etching of substrate 12, thereby forming pores 1514 at a top surface 1524 of substrate 12. In an embodiment, prior to the formation of pores 1514, substrate 12 may be planarized, e.g., by CMP.

Referring to Figure 40C, after the formation of pores 1514, a plurality of layers 10 may be formed over porous top surface 1524 of substrate 12, as described with reference to Figure 1A. Layers 10 may include, for example, graded buffer layer 14, relaxed layer 16, and strained layer 18. Pores 1514 define cleave plane 20 in porous layer 1516 of substrate 12.

Referring to Figure 40D, substrate 12 with layers 10 is bonded to handle wafer 50, including semiconductor substrate 54 and dielectric layer 52, as described with reference to Figure 3. Prior to bonding, a dielectric layer may be formed on a top surface of layers 10 to facilitate the bonding process and to serve as an insulator layer in the final substrate structure.

Referring to Figure 40E as well as to Figure 40D, a split is induced at cleave plane 20 by, for example, cleaving porous layer 1516 by a water or an air jet. The split results in the formation of two separate wafers 1570, 1572. One of these wafers (1572) has graded layer 14 and relaxed layer 16 (see Figure 40c) disposed over strained layer 18, with a first portion 1580 of substrate 12 disposed over graded layer 14. First portion 1580 of substrate 12 may be just trace amounts of material surrounding pores 1514. Strained layer 18 is in contact with dielectric layer 52 on semiconductor substrate 54. The other of these wafers (1570) includes a second portion 1582 of substrate 12, including the bulk of substrate 12 with perhaps trace amounts of material surrounding pores 1514.

Referring to Figure 6 as well as to Figure 40E, first portion 1580 of substrate 12 is removed from graded layer 14 by a wet chemical cleaning process utilizing, for example a mixture of hydrogen peroxide (H_2O_2) and HF. Graded layer 14 and relaxed layer 16 are removed in any one of the methods described for the removal of relaxed layer portion 80 with reference to Figures 4 and 5. Removal of graded and relaxed layers 14, 16 results in the formation of SSOI substrate 100.

Referring to Figure 41A, SSOI substrate 100 (see Figure 6) may also be formed by the use of porous intermediate layers. For example, plurality of layers 10 may be formed over substrate 12, layers 10 including graded layer 14, relaxed layer 16, and strained layer 18 (see Figure 1A). Prior to the formation of strained layer 18, a plurality of pores 1614 may be formed in a top portion of relaxed layer 16, thereby defining a porous layer 1616 in a top portion 1617 of relaxed layer 16. Pores 1614 may be formed by the methods described above with reference to the formation of pores 1514 in Figure 40B. Porous layer 1616 may have a thickness T_{16} of, e.g., 1 - 5 μm. Strained layer 18 may then be formed directly over porous layer 1616. Pores 1614 define cleave plane 20 in porous layer 1616.

Referring to Figure 41B, in an alternative embodiment, after the formation of porous layer 1616 in a portion of relaxed layer 16, a second relaxed layer 1620 may be formed over relaxed layer 16 including porous layer 1616. Second relaxed layer 1620 may include the same material from which relaxed layer 16 is formed, e.g., uniform $Si_{1-x}Ge_x$ having a Ge content of, for example, 10 - 80 % (i.e., x = 0.1 - 0.8) and having a thickness T_{17} of, e.g., 5 - 100 nm. In some embodiments, $Si_{1-x}Ge_x$ may include $Si_{0.70}Ge_{0.30}$ and T_{17} may be approximately 50 nm. Second relaxed layer 1620 may be fully relaxed, as determined by triple axis X-ray diffraction, and may have a threading dislocation density of $<1 \times 10^6$ /cm^2, as determined by etch pit density (EPD) analysis. Strained layer 18 may be formed over second relaxed layer 1620. Pores 1614 define cleave plane 20 in porous layer 1616.

Referring to Figure 41C, substrate 12 with layers 10 is bonded to handle wafer 50, including semiconductor substrate 54 and dielectric layer 52, as described with reference to Figure 3.

Referring to Figure 41D as well as to Figure 41C, a split is induced at cleave plane 20 by, for example, cleaving porous layer 1616 by a water or an air jet. The split results in the formation of two separate wafers 1670, 1672. One of these wafers (1670) has top portion 1617 of relaxed layer 16 (see Figure 41A) disposed over strained layer 18. Strained layer 18 is in

contact with dielectric layer 52 on semiconductor substrate 54. The other of these wafers (1672) includes the substrate 12, graded layer 14, and a bottom portion 1674 of relaxed layer 16.

Referring to Figure 6 as well as to Figure 41D, top portion 1617 of relaxed layer 16 is removed in any one of the methods described for the removal of relaxed layer portion 80 with reference to Figures 4 and 5. Removal of top portion 1617 of relaxed layer 16 results in the formation of SSOI substrate 100.

The bonding of strained silicon layer 18 to dielectric layer 52 has been experimentally demonstrated. For example, strained layer 18 having a thickness of 54 nanometers (nm) along with ~350 nm of $Si_{0.70}Ge_{0.30}$ have been transferred by hydrogen exfoliation to Si handle wafer 50 having dielectric layer 52 formed from thermal SiO_2 with a thickness of approximately 100 nm. The implant conditions were a dose of 4×10^{16} ions/cm^3 of H_2^+ at 75 keV. The anneal procedure was 1 hour at 550 °C to split the SiGe layer, followed by a 1 hour, 800 °C strengthening anneal. The integrity of strained Si layer 18 and good bonding to dielectric layer 52 after layer transfer and anneal were confirmed with cross-sectional transmission electron microscopy (XTEM). An SSOI structure 100 was characterized by XTEM and analyzed via Raman spectroscopy to determine the strain level of the transferred strained Si layer 18. An XTEM image of the transferred intermediate SiGe/strained Si/SiO_2 structure showed transfer of the 54 nm strained Si layer 18 and ~350 nm of the $Si_{0.70}Ge_{0.30}$ relaxed layer 16. Strained Si layer 18 had a good integrity and bonded well to SiO_2 54 layer after the annealing process.

XTEM micrographs confirmed the complete removal of relaxed SiGe layer 16 after oxidation and HF etching. The final structure includes strained Si layer 18 having a thickness of 49 nm on dielectric layer 52 including SiO_2 and having a thickness of 100 nm.

Raman spectroscopy data enabled a comparison of the bonded and cleaved structure before and after SiGe layer 16 removal. Based on peak positions the compostion of the relaxed SiGe layer and strain in the Si layer may be calculated. See, for example, J. C. Tsang, *et al.*, J. Appl. Phys. 75 (12) p. 8098 (1994), incorporated herein by reference. The fabricated SSOI structure 100 had a clear strained Si peak visible at ~511/cm. Thus, the SSOI structure 100 maintained greater than 1% tensile strain in the absence of the relaxed SiGe layer 16. In addition, the absence of Ge-Ge, Si-Ge, and Si-Si relaxed SiGe Raman peaks in the SSOI structure confirmed the complete removal of SiGe layer 16.

In addition, the thermal stability of the strained Si layer was evaluated after a 3 minute 1000 °C rapid thermal anneal (RTA) to simulate an aggregate thermal budget of a CMOS

process. A Raman spectroscopy comparision was made of SSOI structure 100 as processed and after the RTA step. A scan of the as-bonded and cleaved sample prior to SiGe layer removal was used for comparision. Throughout the SSOI structure 100 fabrication processs and subsequent anneal, the strained Si peak was visible and the peak position did not shift. Thus, the strain in SSOI structure 100 was stable and was not diminished by thermal processing. Furthermore, bubbles or flaking of the strained Si surface 18 were not observed by Nomarski optical microscopy after the RTA, indicating good mechanical stability of SSOI structure 100.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The foregoing embodiments are therefore to be considered in all respects illustrative rather than limiting on the invention described herein. Scope of the invention is thus indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein.

What is claimed is:

1. A structure comprising:

a first substrate having a dielectric layer disposed thereon; and

a first strained semiconductor layer disposed in contact with the dielectric layer.

2. The structure of claim 1 wherein the strained semiconductor layer comprises at least one of a group II, a group III, a group IV, a group V, and a group VI element.

3. The structure of claim 2, wherein the strained semiconductor layer comprises silicon.

4. The structure of claim 3, wherein the strained semiconductor layer is substantially free of germanium, and any other layer disposed in contact with the strained semiconductor layer is substantially free of germanium.

5. The structure of claim 2, wherein the strained semiconductor layer comprises germanium.

6. The structure of claim 2, wherein the strained semiconductor layer comprises silicon germanium.

7. The structure of claim 2, wherein the strained semiconductor layer comprises gallium arsenide.

8. The structure of claim 2, wherein the strained semiconductor layer comprises indium phosphide.

9. The structure of claim 2, wherein the strained semiconductor layer comprises zinc selenide.

10. The structure of claim 1, wherein the strained semiconductor layer is tensilely strained.

11. The structure of claim 1, wherein the strained semiconductor layer is compressively strained.

12. The structure of claim 1, wherein the strained semiconductor layer comprises a strained portion and a relaxed portion.

13. The structure of claim 1, further comprising:

a second strained semiconductor layer in contact with the first strained semiconductor layer.

14. The structure of claim 13, wherein the first strained semiconductor layer is compressively strained and the second strained semiconductor layer is tensilely strained.

15. The structure of claim 13, wherein the first strained semiconductor layer is tensilely strained and the second strained semiconductor layer is compressively strained.

16. The structure of claim 1, further comprising:

a transistor including

a source region and a drain region disposed in a portion of the strained semiconductor layer;

a gate disposed above the strained semiconductor layer and between the source and drain regions; and

a gate dielectric layer disposed between the gate and the strained semiconductor layer.

17. The structure of claim 1, wherein the strained semiconductor layer has been formed on a second substrate, has been disposed in contact with the dielectric layer by bonding, and has a lower dislocation density than an initial dislocation density of the strained semiconductor layer as formed.

18. The structure of claim 17, wherein the initial dislocation density has been lowered by etching.

19. The structure of claim 1, wherein the strained semiconductor layer has been grown with an initial dislocation density and has a dislocation density less than the initial dislocation density.

20. The structure of claim 1, wherein the strained semiconductor layer has been formed by epitaxy.

21. The structure of claim 1, wherein the strained semiconductor layer has a thickness uniformity of better than approximately ±5%.

22. The structure of claim 1, wherein the strained layer has a thickness selected from a range of approximately 20 angstroms - 1000 angstroms.

23. The structure of claim 1, wherein the strained layer has a surface roughness of less than approximately 20 angstroms.

24. The structure of claim 1, wherein the substrate comprises silicon.

25. The structure of claim 1, wherein the substrate comprises germanium.

26. The structure of claim 1, wherein the substrate comprises silicon germanium.

27. A structure comprising:

a relaxed substrate comprising a bulk material; and

a strained layer disposed in contact with the relaxed substrate,

wherein the strain of the strained layer is not induced by the underlying substrate and the strain is independent of a lattice mismatch between the strained layer and the relaxed substrate.

28. The structure of claim 27, wherein the bulk material comprises a first semiconductor material.

29. The structure of claim 27, wherein the strained layer comprises a second semiconductor material.

30. The structure of claim 29, wherein the bulk material comprises a first semiconductor material.

31. The structure of claim 30, wherein the first semiconductor material is essentially the same as the second semiconductor material.

32. The structure of claim 31, wherein the first semiconductor material and the second semiconductor material comprise silicon.

33. The structure of claim 27, wherein a lattice constant of the relaxed substrate is equal to a lattice constant of the strained layer in the absence of said strain.

34. The structure of claim 27, wherein the strain of the strained layer is greater than approximately 1×10^{-3}.

35. The structure of claim 27, wherein the strained layer has been formed by epitaxy.

36. The structure of claim 27, wherein the strained layer has a thickness uniformity of better than approximately ±5%.

37. The structure of claim 27, wherein the strained layer has a thickness selected from a range of approximately 20 angstroms - 1000 angstroms.

38. The structure of claim 27, wherein the strained layer has a surface roughness of less than approximately 20 angstroms.

39. The structure of claim 27, further comprising:

a transistor including

a source region and a drain region disposed in a portion of the strained semiconductor layer;

a gate contact disposed above the strained semiconductor layer and between the source and drain regions; and

a gate dielectric layer disposed between the gate contact and the strained semiconductor layer.

40. A structure comprising:

a substrate comprising a dielectric material; and

a strained semiconductor layer disposed in contact with the dielectric material.

41. The structure of claim 40, wherein the dielectric material comprises sapphire.

42. The structure of claim 40, wherein the semiconductor layer has been formed on a second substrate, has been disposed in contact with the dielectric material by bonding, and has a lower dislocation density than an initial dislocation density of the semiconductor layer as formed.

43. The structure of claim 42, wherein the initial dislocation density has been lowered by etching.

44. The structure of claim 40, wherein the semiconductor layer has been formed by epitaxy.

45. A method for forming a structure, the method comprising:

providing a first substrate having a first strained semiconductor layer formed thereon;

bonding the first strained semiconductor layer to an insulator layer disposed on a second substrate; and

removing the first substrate from the first strained semiconductor layer, the strained semiconductor layer remaining bonded to the insulator layer.

46. The method of claim 45, wherein the strained semiconductor layer is tensilely strained.

47. The method of claim 45, wherein the strained semiconductor layer is compressively strained.

48. The method of claim 45, wherein the strained semiconductor layer comprises a surface layer after the removal of the first substrate.

49. The method of claim 45, wherein the strained semiconductor layer comprises a buried layer after the removal of the first substrate.

50. The method of claim 45, wherein removing the first substrate from the strained semiconductor layer comprises cleaving.

51. The method of claim 50, wherein cleaving comprises implantation of an exfoliation species through the strained semiconductor layer to initiate cleaving.

52. The method of claim 51, wherein the exfoliation species comprises at least one of hydrogen and helium.

53. The method of claim 50, wherein providing the first substrate comprises providing the first substrate having a second strained layer disposed between the substrate and the first strained layer, the second strained layer acting as a cleave plane during cleaving.

54. The method of claim 53, wherein the second strained layer comprises a compressively strained layer.

55. The method of claim 54, wherein the compressively strained layer comprises $Si_{1-x}Ge_x$.

56. The method of claim 45, wherein providing the first substrate comprises providing the first substrate having a relaxed layer disposed between the substrate and the first strained layer.

57. The method of claim 56, further comprising:
planarizing the relaxed layer prior to forming the first strained semiconductor layer.

58. The method of claim 57, further comprising:
after planarizing the relaxed layer, forming a relaxed semiconductor regrowth layer thereon.

59. The method of claim 45, further comprising:
forming a dielectric layer over the first strained semiconductor layer prior to bonding the first strained semiconductor layer to an insulator layer.

60. The method of claim 45, wherein removing the first substrate from the strained semiconductor layer comprises mechanical grinding.

61. The method of claim 45, wherein bonding comprises achieving a high bond strength at a low temperature.

62. The method of claim 61, wherein the bond strength is greater than or equal to about 1000 milliJoules/meter squared (mJ/m^2).

63. The method of claim 61, wherein the temperature is less than approximately 600 °C.

64. The method of claim 61, wherein bonding comprises plasma activation of a surface of the first semiconductor layer prior to bonding the first semiconductor layer.

65. The method of claim 64, wherein plasma activation comprises use of at least one of an ammonia (NH_3), an oxygen (O_2), an argon (Ar), and a nitrogen (N_2) source gas.

66. The method of claim 61, wherein bonding comprises planarizing a surface of the first semiconductor layer prior to bonding the first semiconductor layer.

67. The method of claim 66, wherein planarizing comprises chemical-mechanical polishing.

68. The method of claim 45, further comprising:
relaxing a portion of the first strained semiconductor layer.

69. The method of claim 68, wherein the portion of the first strained semiconductor layer is relaxed by introducing a plurality of ions into the portion of the first strained semiconductor layer.

70. The method of claim of claim 45, further comprising:

forming a transistor by

forming a gate dielectric layer above a portion of the strained semiconductor layer;

forming a gate contact above the gate dielectric layer; and

forming a source region and a drain region in a portion of the strained semiconductor layer, proximate the gate dielectric layer.

71. A method for forming a structure, the method comprising:

providing a substrate having a relaxed layer disposed over a first strained layer, the relaxed layer inducing strain in the first strained layer; and

removing at least a portion of the relaxed layer selectively with respect to the first strained layer.

72. The method of claim 71, wherein providing the substrate comprises bonding the first strained layer to the substrate.

73. The method of claim 72, wherein the first strained layer is bonded to an insulator layer disposed on the substrate.

74. The method of claim 71, further comprising:

before providing the substrate, forming the first strained layer over the relaxed layer on another substrate.

75. The method of claim 71, wherein the portion of the relaxed layer is removed by oxidation.

76. The method of claim 71, wherein the portion of the relaxed layer is removed by a wet chemical etch.

77. The method of claim 71, wherein the portion of the relaxed layer is removed by a dry etch.

78. The method of claim 71, wherein the portion of the relaxed layer is removed by chemical-mechanical polishing.

79. The method of claim 71, further comprising:
after removal of at least a portion of the relaxed layer, planarizing the strained layer.

80. The method of claim 79, wherein planarizing the strained layer comprises chemical-mechanical polishing.

81. The method of claim 79, wherein planarizing the strained layer comprises an anneal.

82. The method of claim 81, wherein the anneal is performed at a temperature greater than 800 °C.

83. The method of claim 71, wherein providing the substrate comprises providing the substrate having an etch stop layer disposed between the relaxed layer and the strained layer.

84. The method of claim 83, wherein the etch stop layer is compressively strained.

85. The method of claim 83, wherein the strained layer comprises silicon, the relaxed layer comprises silicon germanium, and the etch stop layer comprises silicon germanium carbon.

86. The method of claim 83, wherein the relaxed layer comprises $Si_{1-y}Ge_y$, the etch stop layer comprises $Si_{1-x}Ge_x$, and x is greater than y.

87. The method of claim 86, wherein x is approximately 0.5 and y is approximately 0.2.

88. The method of claim 83, wherein the etch stop layer enables an etch selectivity to the relaxed layer of greater than 10:1.

89. The method of claim 88, wherein the etch stop layer enables an etch selectivity to the relaxed layer of greater than 100:1.

90. The method of claim 83, wherein the etch stop layer has a thickness selected from a range of about 20 angstroms to about 1000 angstroms.

91. The method of claim 71, wherein providing the substrate comprises forming the relaxed layer over a graded layer.

92. A method for forming a structure, the method comprising:

providing a first substrate having a dielectric layer disposed thereon;

forming a semiconductor layer on a second substrate, the semiconductor layer having an initial misfit dislocation density;

bonding the semiconductor layer to the dielectric layer;

removing the second substrate, the semiconductor layer remaining bonded to the dielectric layer; and

reducing the misfit dislocation density in the semiconductor layer.

93. The method of claim 92, wherein the misfit dislocation density is reduced by removing a portion of the semiconductor layer.

94. The method of claim 93, wherein the portion of the semiconductor layer is removed by etching.

95. The method of claim 93, further comprising:

after removing a portion of the semiconductor layer to reduce misfit dislocation density, forming a regrowth layer over the semiconductor layer without increasing misfit dislocation density.

96. The method of claim 95, wherein the regrowth layer is formed by epitaxy.

97. A method for forming a structure, the method comprising:

providing a first substrate having a dielectric layer disposed thereon;

forming a semiconductor layer on a second substrate, the semiconductor layer having an initial misfit dislocation density;

bonding the semiconductor layer to the dielectric layer;

removing the second substrate, the semiconductor layer remaining bonded to the dielectric layer; and

growing a regrowth layer over the semiconductor layer.

98. The method of claim 97, wherein the semiconductor layer and the regrowth layer comprise the same semiconductor material.

99. The method of claim 97, wherein the semiconductor layer and the regrowth layer together have a misfit dislocation density not greater than the initial misfit dislocation density.

100. A method for forming a structure, the method comprising:

providing a first substrate having a strained layer disposed thereon, the strained layer including a first semiconductor material;

bonding the strained layer to a second substrate, the second substrate comprising a bulk material; and

removing the first substrate from the strained layer, the strained layer remaining bonded to the bulk semiconductor material,

wherein the strain of the strained layer is not induced by the second substrate and the strain is independent of lattice mismatch between the strained layer and the second substrate.

101. The method of claim 100, wherein the bulk material comprises a second semiconductor material.

102. The method of claim 101, wherein the first semiconductor material is substantially the same as the second semiconductor material.

103. The method of claim 100, wherein the second substrate comprises silicon.

104. The method of claim 100, wherein the strained semiconductor layer comprises silicon.

105. A method for forming a structure, the method comprising:

providing a first substrate having a semiconductor layer disposed over a strained layer;

bonding the semiconductor layer to an insulator layer disposed on a second substrate; and

removing the first substrate from the strained layer, the semiconductor layer remaining bonded to the insulator layer.

106. The method of claim 105, wherein the semiconductor layer is substantially relaxed.

107. The method of claim 105, wherein the semiconductor layer comprises at least one of a group II, a group III, a group IV, a group V, and a group VI element.

108. The method of claim 105, wherein the strained layer comprises at least one of a group II, a group III, a group IV, a group V, and a group VI element.

109. The method of claim 107, wherein the semiconductor layer comprises germanium and the strained layer comprises silicon.

110. A structure comprising:

a substrate having a dielectric layer disposed thereon; and

a strained semiconductor layer disposed in contact with the dielectric layer,

wherein the semiconductor layer comprises approximately 100% germanium.

111. The structure of claim 110, wherein the strained semiconductor layer is compressively strained.

112. The structure of claim 110, wherein the strained semiconductor layer comprises a thin layer and the thin layer is disposed in contact with the dielectric layer.

113. The structure of claim 112, wherein the thin layer comprises silicon.

114. A structure comprising:

a substrate having a dielectric layer disposed thereon;

a strained semiconductor layer disposed in contact with the dielectric layer; and

a transistor including

a source region and a drain region disposed in a portion of the strained semiconductor layer, and

a gate disposed above the strained semiconductor layer and between the source and drain regions, the gate comprising a material selected from the group consisting of a doped semiconductor, a metal, and a metallic compound.

115. The structure of claim 114, wherein the doped semiconductor comprises a material selected from the group consisting of polycrystalline silicon and polycrystalline silicon-germanium.

116. The structure of claim 114, wherein the metal comprises a material selected from the group consisting of titanium, tungsten, molybdenum, tantalum, nickel, and iridium.

117. The structure of claim 114, wherein the metal compound comprises a material selected from the group consisting of titanium nitride, titanium silicon nitride, tungsten nitride, tantalum nitride, tantalum silicide, nickel silicide, and iridium oxide.

118. The structure of claim 114, further comprising:

a contact layer disposed over at least a portion of the strained semiconductor layer,

wherein a bottommost boundary of the contact layer is disposed above a bottommost boundary of the strained semiconductor layer.

119. The structure of claim 118, wherein the bottommost boundary of the contact layer shares an interface with the strained semiconductor layer.

120. A structure comprising:

a substrate having a dielectric layer disposed thereon, the dielectric layer having a melting point greater than about 1700°C; and

a first strained semiconductor layer disposed in contact with the dielectric layer.

121. The structure of claim 120, wherein the dielectric layer comprises a material selected from the group consisting of aluminum oxide, magnesium oxide, and silicon nitride.

122. A structure comprising:

a substrate having a dielectric layer disposed thereon; and

a strained semiconductor layer disposed in contact with the dielectric layer,

wherein the strained semiconductor layer comprises approximately 100% silicon and has a misfit dislocation density of less than about 10^5 cm/cm^2.

123. A structure comprising:

a substrate having a dielectric layer disposed thereon; and

a strained semiconductor layer disposed in contact with the dielectric layer,

wherein the strained semiconductor layer comprises approximately 100% silicon and has a threading dislocation density selected from the range of about 10 dislocations/cm^2 to about 10^7 dislocations/cm^2.

124. A structure comprising:

a substrate having a dielectric layer disposed thereon; and

a strained semiconductor layer disposed in contact with the dielectric layer,

wherein the semiconductor layer comprises approximately 100% silicon and has a surface roughness selected from the range of approximately 0.01 nm to approximately 1 nm.

125. A structure comprising:

a substrate having a dielectric layer disposed thereon; and

a strained semiconductor layer disposed in contact with the dielectric layer,

wherein the strained semiconductor layer comprises approximately 100% silicon and has a thickness uniformity across the substrate of better than approximately ±10%.

126. A structure comprising:

a substrate having a dielectric layer disposed thereon; and

a strained semiconductor layer disposed in contact with the dielectric layer,

wherein the strained semiconductor layer comprises approximately 100% silicon and has a thickness of less than approximately 200 Å.

127. A structure comprising:

a substrate having a dielectric layer disposed thereon; and

a strained semiconductor layer disposed in contact with the dielectric layer,

wherein the semiconductor layer comprises approximately 100% silicon and has a surface germanium concentration of less than approximately $1x10^{12}$ atoms/cm^2.

128. A structure comprising:

a substrate having a dielectric layer disposed thereon; and

a strained semiconductor layer disposed in contact with the dielectric layer,

wherein an interface between the strained semiconductor layer and the dielectric layer has a density of bonding voids of less than 0.3 voids/cm^2.

129. A method for forming a structure, the method comprising:

providing a first substrate comprising a porous layer defining a cleave plane and having a first strained semiconductor layer formed thereon;

bonding the first strained semiconductor layer to an insulator layer disposed on a second substrate; and

removing the first substrate from the first strained semiconductor layer by cleaving at the cleave plane, the strained semiconductor layer remaining bonded to the insulator layer.

130. A method for forming a structure, the method comprising:

forming a first relaxed layer over a first substrate, wherein the first relaxed layer includes a porous layer defining a cleave plane;

forming a strained semiconductor layer over the first relaxed layer;

bonding the first strained semiconductor layer to an insulator layer disposed on a second substrate; and

removing the first substrate from the strained semiconductor layer by cleaving at the cleave plane, the strained semiconductor layer remaining bonded to the insulator layer.

131. The method of claim 130, wherein the porous layer is disposed at a top portion of the first relaxed layer.

132. The method of claim 130, further comprising:

forming a second relaxed layer over the first relaxed layer,

wherein the strained semiconductor layer is formed over the second relaxed layer.

133. The method of claim 132, further comprising:

planarizing the first relaxed layer prior to forming the second relaxed layer.

134. The method of claim 133, wherein planarizing comprises chemical-mechanical polishing.

135. The method of claim 130, wherein at least a portion of the porous layer remains disposed on the first strained semiconductor layer after cleaving.

136. The method of claim 135, further comprising:

removing the portion of the porous layer from the strained semiconductor layer after cleaving.

137. The method of claim 136, wherein removing the portion of the porous layer comprises cleaning the strained semiconductor layer with a wet chemical solution.

138. The method of claim 137, wherein the wet chemical solution comprises hydrogen peroxide.

139. The method of claim 137, wherein the wet chemical solution comprises hydrofluoric acid.

140. The method of claim 136, wherein removing the portion of the porous layer comprises oxidation.

141. A structure comprising:

a substrate having a dielectric layer disposed thereon; and

a fin-field-effect transistor disposed over the substrate, the fin-field-effect-transistor including:

a source region and a drain region disposed in contact with the dielectric layer, the source and the drain regions comprising a strained semiconductor material;

at least one fin extending between the source and the drain regions, the fin comprising a strained semiconductor material;

a gate disposed above the strained semiconductor layer, extending over at least one fin and between the source and the drain regions; and

a gate dielectric layer disposed between the gate and the fin.

142. The structure of claim 141, wherein the fin comprises at least one of a group II, a group III, a group IV, a group V, of a group VI element.

143. The structure of claim 141, wherein the strained semiconductor layer is tensilely strained.

144. The structure of claim 143, wherein the strained semiconductor layer comprises tensilely strained silicon.

145. The structure of claim 141, wherein the strained semiconductor layer is compressively strained.

146. The structure of claim 145, wherein the strained semiconductor layer comprises compressively strained germanium.

147. A method for forming a structure, the method comprising:

providing a substrate having a dielectric layer disposed thereon, and a first strained semiconductor layer disposed in contact with the dielectric layer; and

forming a fin-field-effect transistor on the substrate by:

patterning the first strained semiconductor layer to define a source region, a drain region, and at least one fin disposed between the source and the drain regions,

forming a dielectric layer, at least a portion of the dielectric layer being disposed over the fin, and

forming a gate over the dielectric layer portion disposed over the fin.

148. The method of claim 147 wherein the first strained semiconductor layer comprises at least one of a group II, a group III, a group IV, a group V, or a group VI element.

149. The method of claim 147, wherein the strained semiconductor layer is tensilely strained.

150. The method of claim 149, wherein the strained semiconductor layer comprises tensilely strained silicon.

151. The method of claim 147, wherein the strained semiconductor layer is compressively strained.

152. The method of claim 151, wherein the strained semiconductor layer comprises compressively strained germanium.

153. A structure comprising:

a dielectric layer disposed over a substrate; and

a transistor formed over the dielectric layer, the transistor including:

a first gate electrode in contact with the dielectric layer;

a strained semiconductor layer disposed over the first gate electrode; and

a second gate electrode disposed over the strained semiconductor layer.

154. The structure of claim 153, wherein the strained semiconductor layer comprises at least one of a group II, a group III, a group IV, a group V, and a group VI elements.

155. The structure of claim 153, wherein the strained semiconductor layer is tensilely strained

156. The structure of claim 155, wherein the strained semiconductor layer comprises tensilely strained silicon.

157. The structure of claim 153, wherein the strained semiconductor layer is compressively strained.

158. The structure of claim 157, wherein the strained semiconductor layer comprises compressively strained germanium.

159. The structure of claim 153, wherein the strained semiconductor layer has a strain level greater than 10^{-3}.

160. The structure of claim 153, further comprising:

a first gate insulator layer disposed between the first gate electrode and the strained semiconductor layer.

161. The structure of claim 153, further comprising:

a second gate insulator layer disposed between the strained semiconductor layer and the second gate electrode.

162. The structure of claim 153, wherein the strained semiconductor layer comprises a source.

163. The structure of claim 153, wherein the strained semiconductor layer comprises a drain.

164. The structure of claim 153, further comprising:

a sidewall spacer disposed proximate the second gate electrode.

165. The structure of claim 164, wherein the sidewall spacer comprises a dielectric material.

166. The structure of claim 24, wherein the sidewall spacer comprises a conductive material.

167. A method for forming a structure, the method comprising:

forming a substrate having a first gate electrode layer disposed over a substrate insulator layer, a first gate insulator layer disposed over the first gate electrode layer, and a strained semiconductor layer disposed over the first gate insulator layer;

forming a second gate insulator layer over the strained semiconductor layer;

forming a second gate electrode layer over the second gate insulator layer;

defining a second gate electrode by removing a portion of the second gate insulator layer;

forming a dielectric sidewall spacer proximate the second gate electrode;

removing a portion of the strained semiconductor layer, a portion of the first gate insulator layer, and a portion of the first gate electrode layer to define a vertical structure disposed over the substrate insulator layer, the vertical structure including a strained layer region

a first gate insulator region, and a first gate electrode layer region disposed under the second gate electrode; and

defining a first gate electrode by laterally shrinking the first gate electrode layer region.

168. The method of claim 167, wherein the strained semiconductor layer is tensilely strained.

169. The method of claim 168, wherein the strained semiconductor layer comprises tensilely strained silicon.

170. The method of claim 167, wherein the strained semiconductor layer is compressively strained.

171. The method of claim 170, wherein the strained semiconductor layer comprises compressively strained germanium.

172. The method of claim 167, further comprising:

forming a conductive sidewall spacer proximate the dielectric sidewall spacer.

173. The method of claim 167, further comprising:

defining a source in the strained semiconductor layer.

174. The method of claim 167, further comprising:

defining a drain in the strained semiconductor layer.

175. A structure comprising:

a strained semiconductor layer disposed over a dielectric layer; and

a bipolar transistor including:

a collector disposed in a portion of the strained semiconductor layer,

a base disposed over the collector, and

an emitter disposed over the base.

176. The structure of claim 175, wherein the strained layer is tensilely strained.

177. The structure of claim 176, wherein the strained layer comprises tensilely strained silicon.

178. The structure of claim 175, wherein the strained layer is compressively strained.

179. A structure comprising:

a relaxed substrate comprising a bulk material;

a strained layer disposed in contact with the relaxed substrate; and

a bipolar transistor including:

a collector disposed in a portion of the strained layer,

a base disposed over the collector, and

an emitter disposed over the base,

wherein the strain of the strained layer is not induced by the underlying substrate.

180. The structure of claim 179, wherein the strained layer is tensilely strained.

181. The structure of claim 180, wherein the strained layer comprises tensilely strained silicon.

182. The structure of claim 179, wherein the strained layer is compressively strained.

183. A structure comprising:

a relaxed substrate comprising a bulk material;

a strained layer disposed in contact with the relaxed substrate; and

a bipolar transistor including:

a collector disposed in a portion of the strained layer,

a base disposed over the collector, and

an emitter disposed over the base,

wherein the strain of the strained layer is independent of a lattice mismatch between the strained layer and the relaxed substrate.

184. The structure of claim 183, wherein the strained layer is tensilely strained.

185. The structure of claim 184, wherein the strained layer comprises tensilely strained silicon.

186. The structure of claim 183, wherein the strained layer is compressively strained.

187. A method for forming a structure, the method comprising:

providing a substrate having a strained semiconductor layer disposed over a dielectric layer;

defining a collector in a portion of the strained semiconductor layer;

forming a base over the collector; and

forming an emitter over the base.

188. The structure of claim 187, wherein the strained semiconductor layer is tensilely strained.

189. The structure of claim 188, wherein the strained semiconductor layer comprises tensilely strained silicon.

190. The structure of claim 187, wherein the strained semiconductor layer is compressively strained.

191. A method for forming a structure, the method comprising:

providing a first substrate having a strained layer disposed thereon, wherein the strained layer includes a first semiconductor material;

bonding the strained layer to a second substrate, wherein the second substrate comprises a bulk material;

removing the first substrate from the strained layer, the strained layer remaining bonded to the bulk semiconductor material;

defining a collector in a portion of the strained layer;

forming a base over the collector; and

forming an emitter over the base,

wherein the strain of the strained layer is not induced by the second substrate and the strain is independent of lattice mismatch between the strained layer and the second substrate.

192. The structure of claim 191, wherein the strained layer is tensilely strained.

193. The structure of claim 192 wherein the strained layer comprises tensilely strained silicon.

194. The structure of claim 187 wherein the strained layer is compressively strained.

195. A method for forming a structure, the method comprising:

providing a relaxed substrate comprising a bulk material and a strained layer disposed in contact with the relaxed substrate, the strain of the strained layer not being induced by the underlying substrate and the strain being independent of a lattice mismatch between the strained layer and the relaxed substrate;

defining a collector in a portion of the strained layer;

forming a base over the collector; and

forming an emitter over the base.

196. The structure of claim 195, wherein the strained layer is tensilely strained.

197. The structure of claim 196, wherein the strained layer comprises tensilely strained silicon.

198. The structure of claim 195 wherein the strained layer is compressively strained.

199. A method for forming a structure, the method comprising:

providing a substrate having a strained semiconductor layer disposed over a substrate dielectric layer;

forming a transistor in the strained layer by

forming a gate dielectric layer above a portion of the strained semiconductor layer,

forming a gate contact above the gate dielectric layer, and

forming a source region and a drain region in a portion of the strained semiconductor layer, proximate the gate dielectric layer;

removing a portion of the strained layer and the substrate dielectric layer to expose a portion of the substrate;

defining a collector in the exposed portion of the substrate;

forming a base over the collector; and

forming an emitter over the base.

200. The structure of claim 199, wherein the strained layer is tensilely strained.

201. The structure of claim 200, wherein the strained layer comprises tensilely strained silicon.

202. The structure of claim 199, wherein the strained layer is compressively strained.

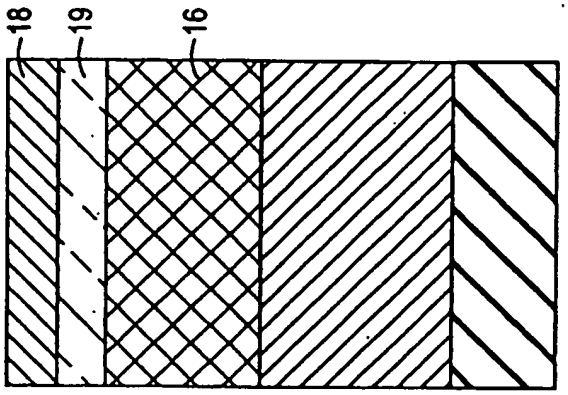

FIG. 1B

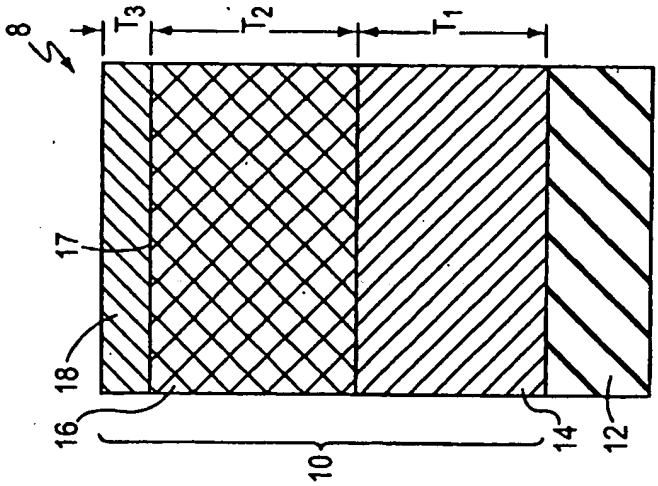

FIG. 1A

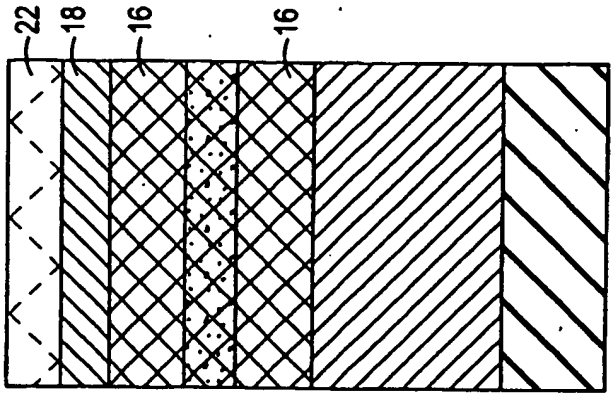

FIG. 2B

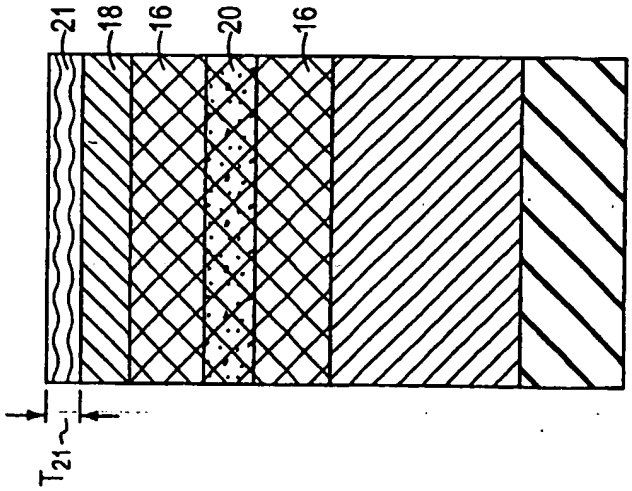

FIG. 2A

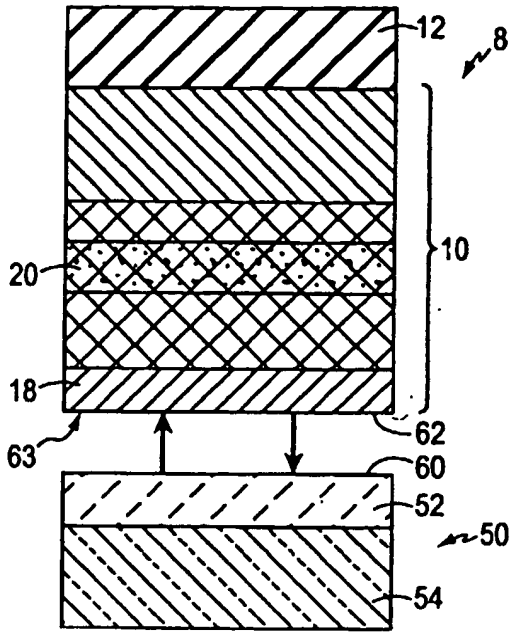

FIG. 3

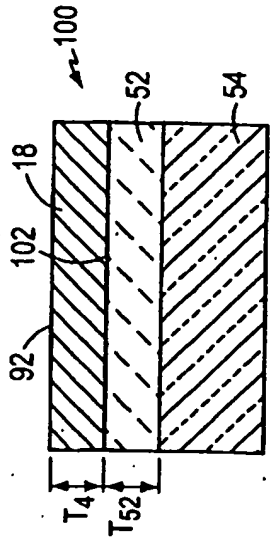

FIG. 6

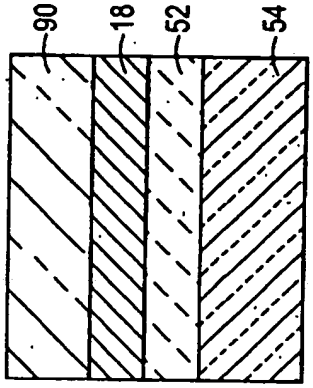

FIG. 5

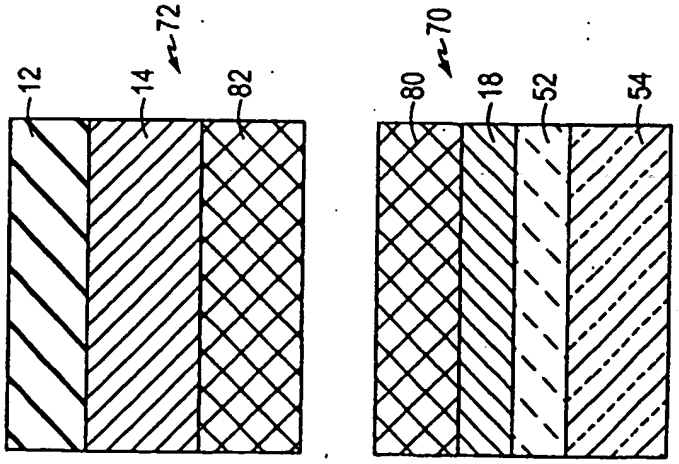

FIG. 4

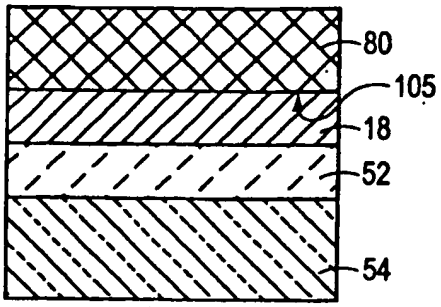

FIG. 7

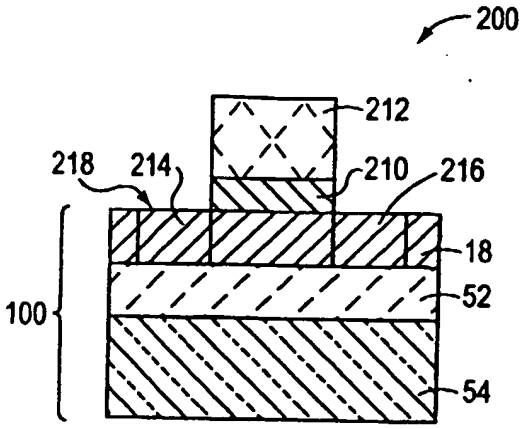

FIG. 8A

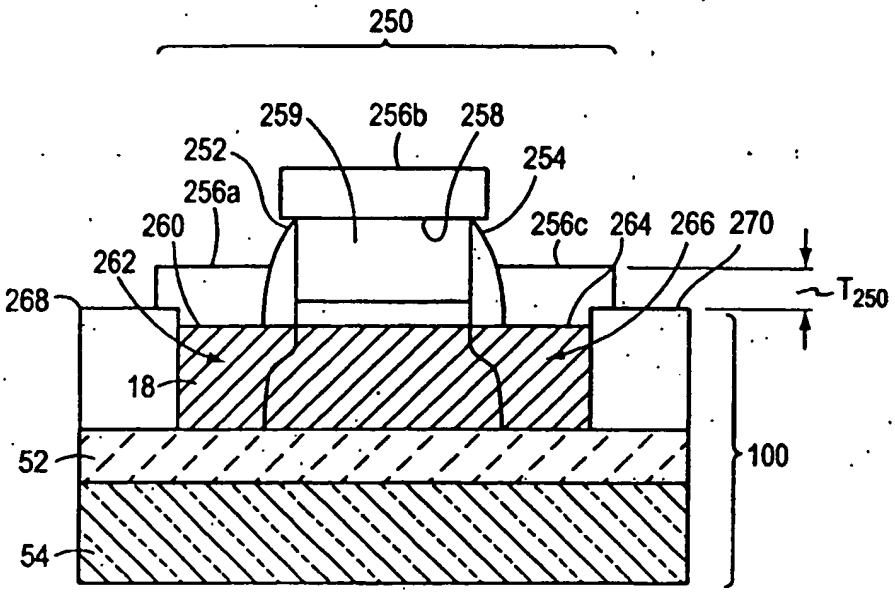
250
259
256b
258
252
254
256a
260
256c
264
266
270
262
268
T_{250}
18
52
100
54

FIG. 8B

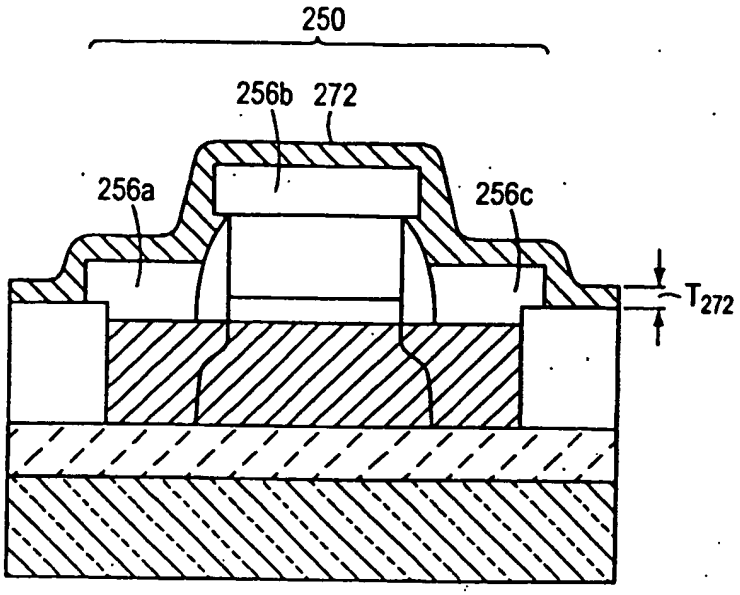

FIG. 8C

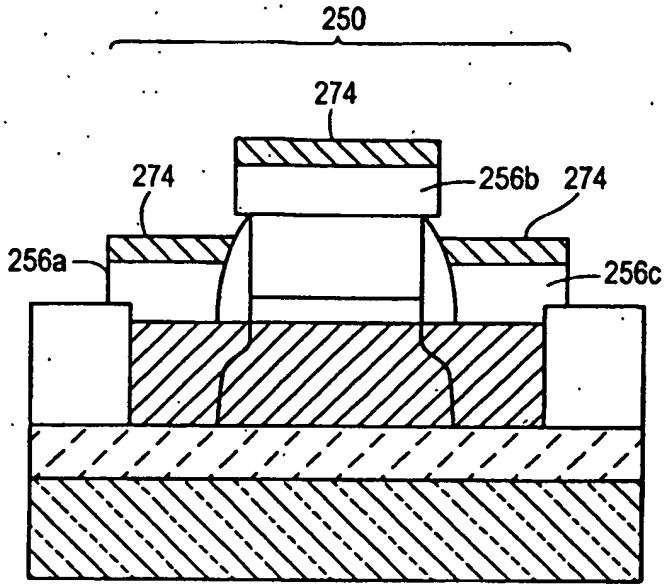

FIG. 8D

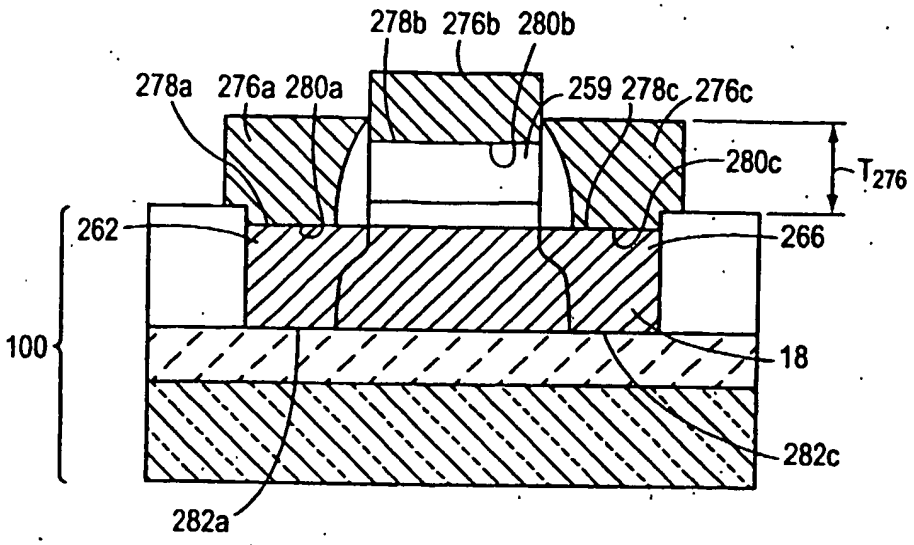
278b
276b
280b
278a
276a
280a
259
278c
276c
280c
T_{276}
262
266
100
18
282c
282a

FIG. 8E

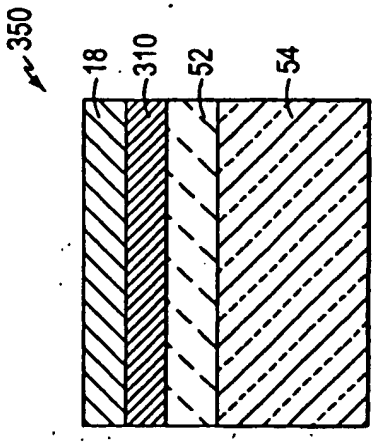

FIG. 10

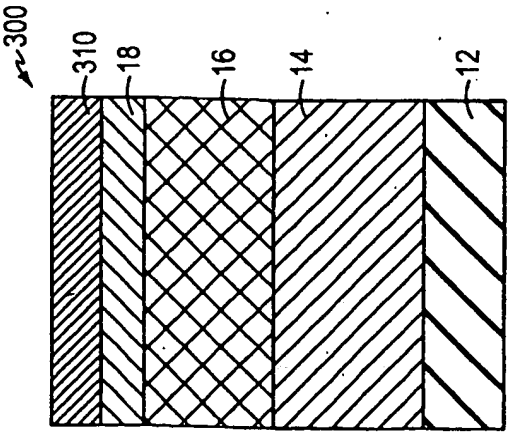

FIG. 9

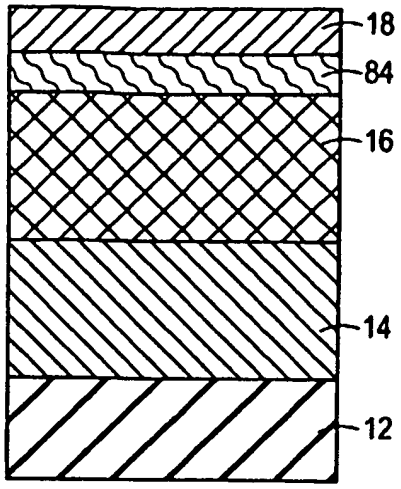

FIG. 11

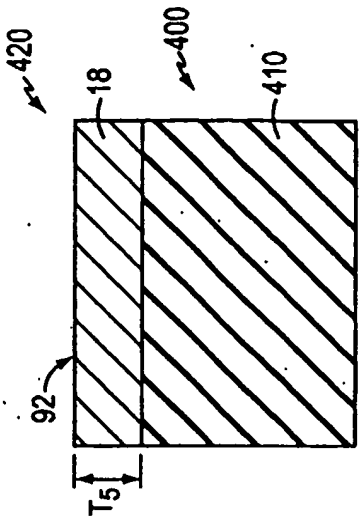

FIG. 13

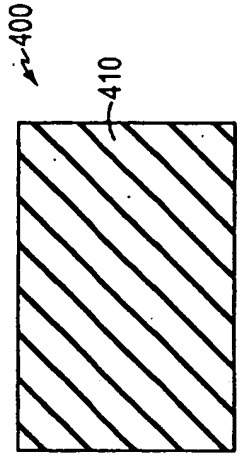

FIG. 12

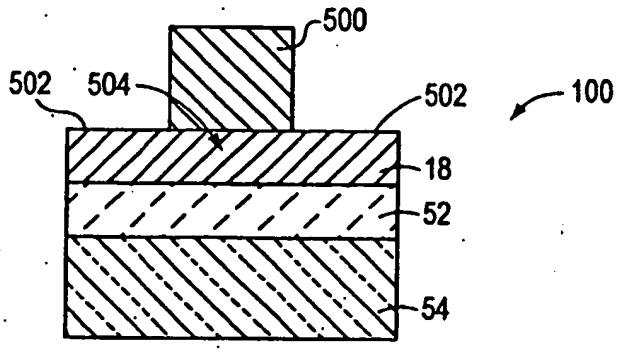

FIG. 14

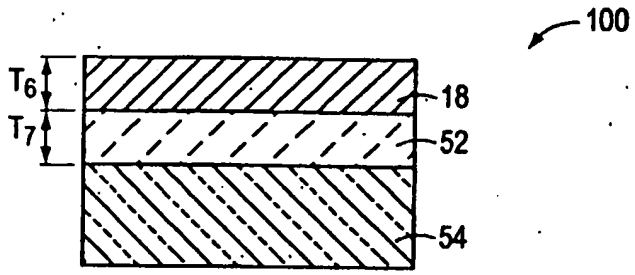

FIG. 15

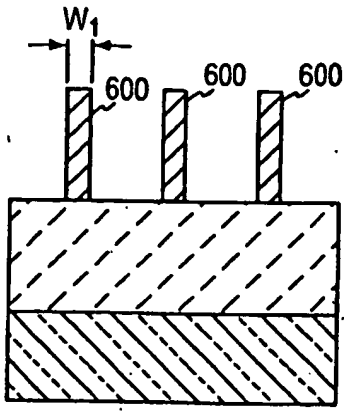

FIG. 16A

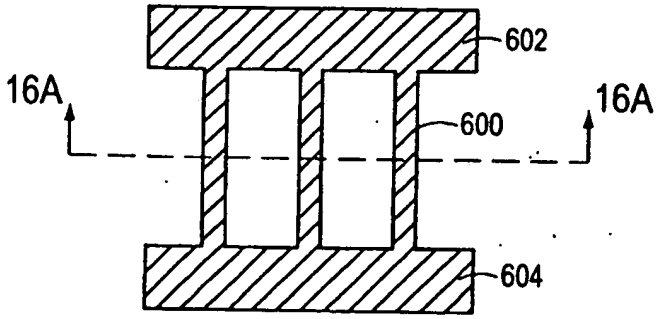

FIG. 16B

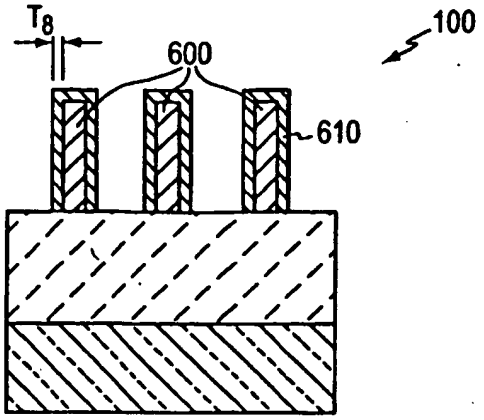

FIG. 17

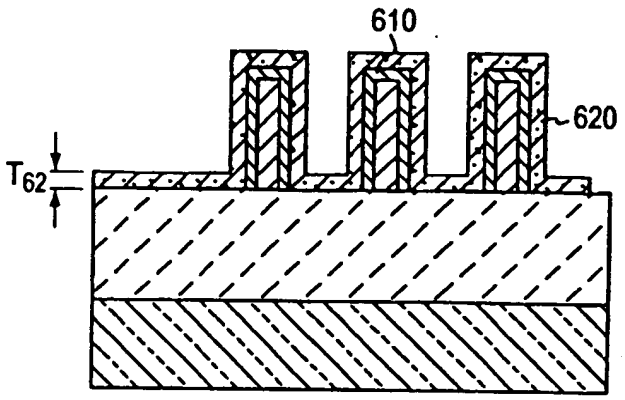

FIG. 18A

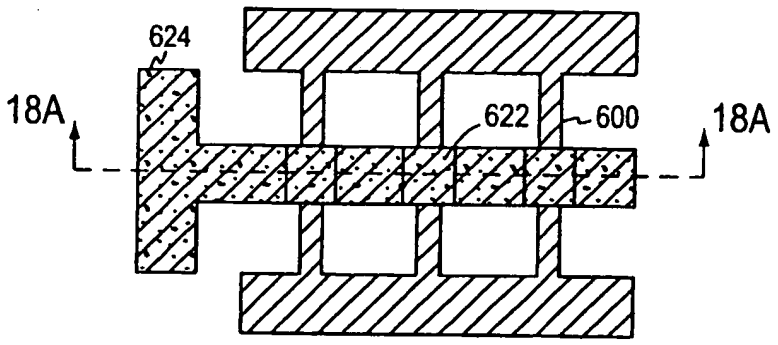

FIG. 18B

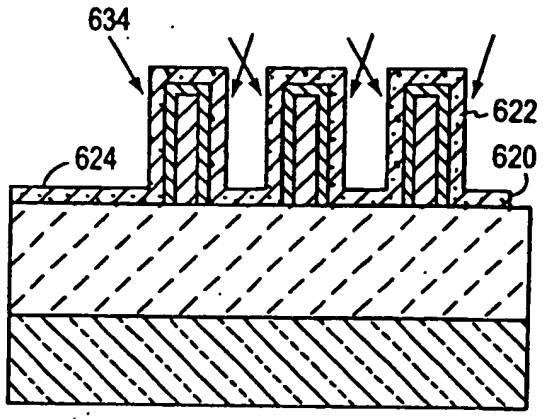

FIG. 19A

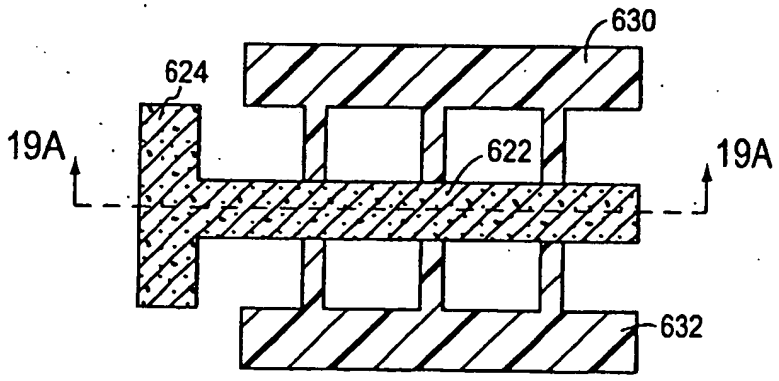

FIG. 19B

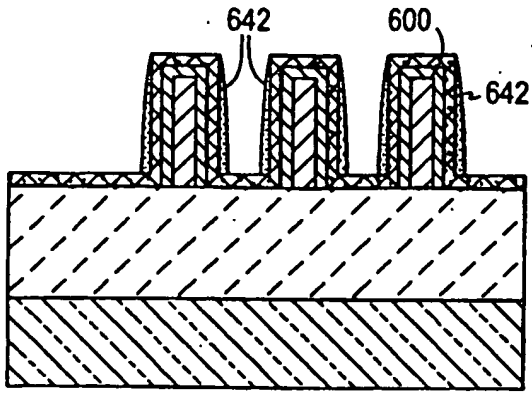

FIG. 20A

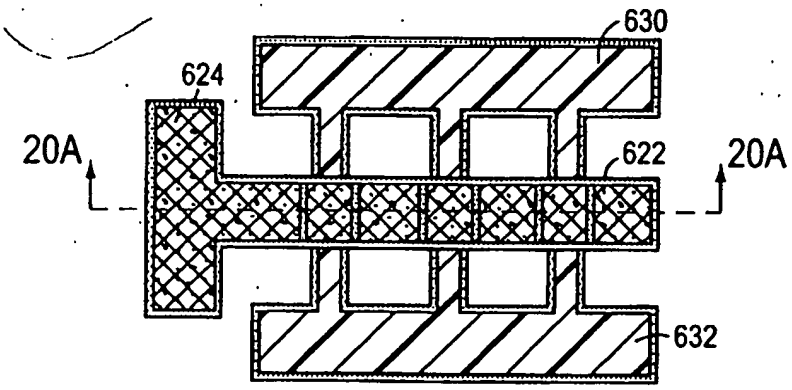

FIG. 20B

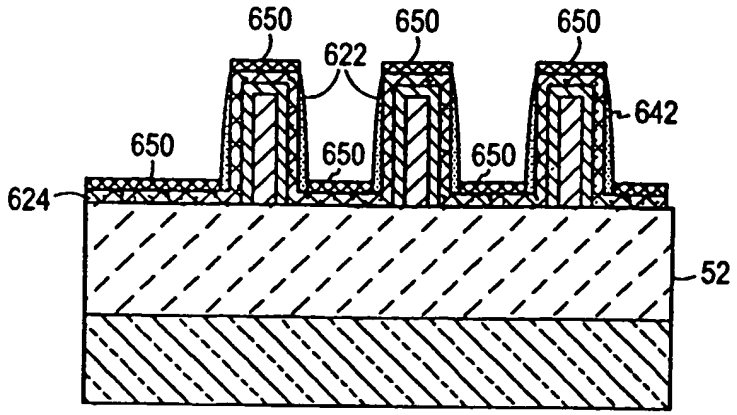

FIG. 21A

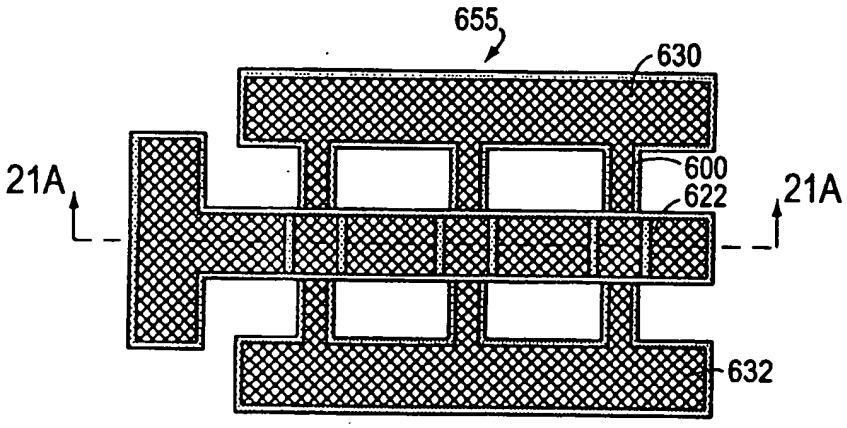

FIG. 21B

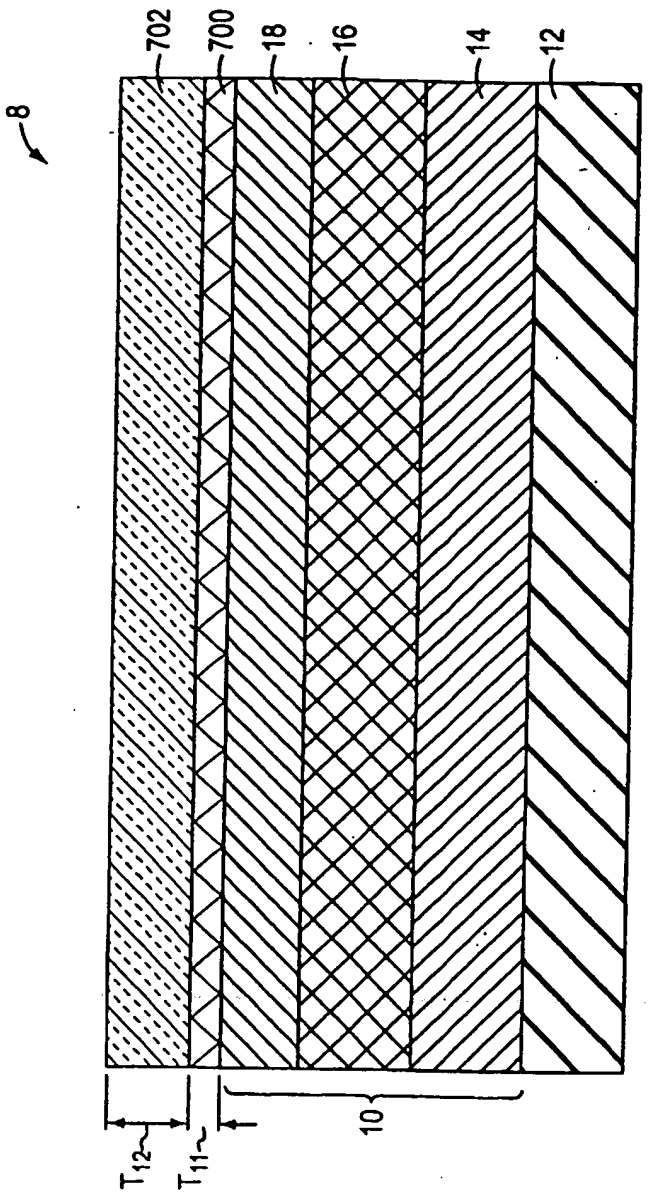

FIG. 22

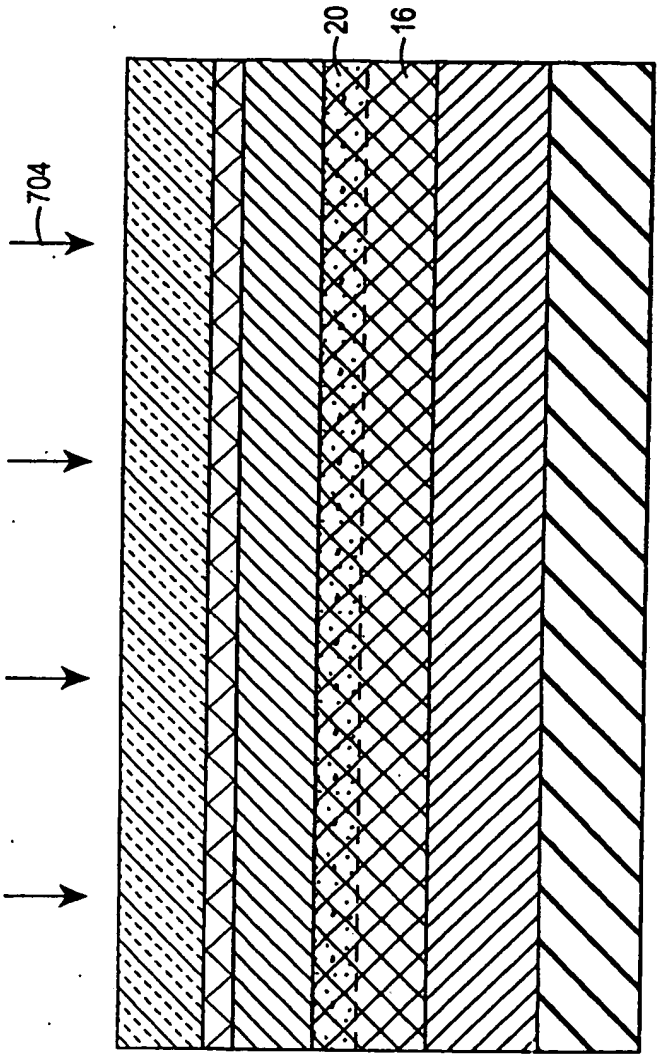

FIG. 23

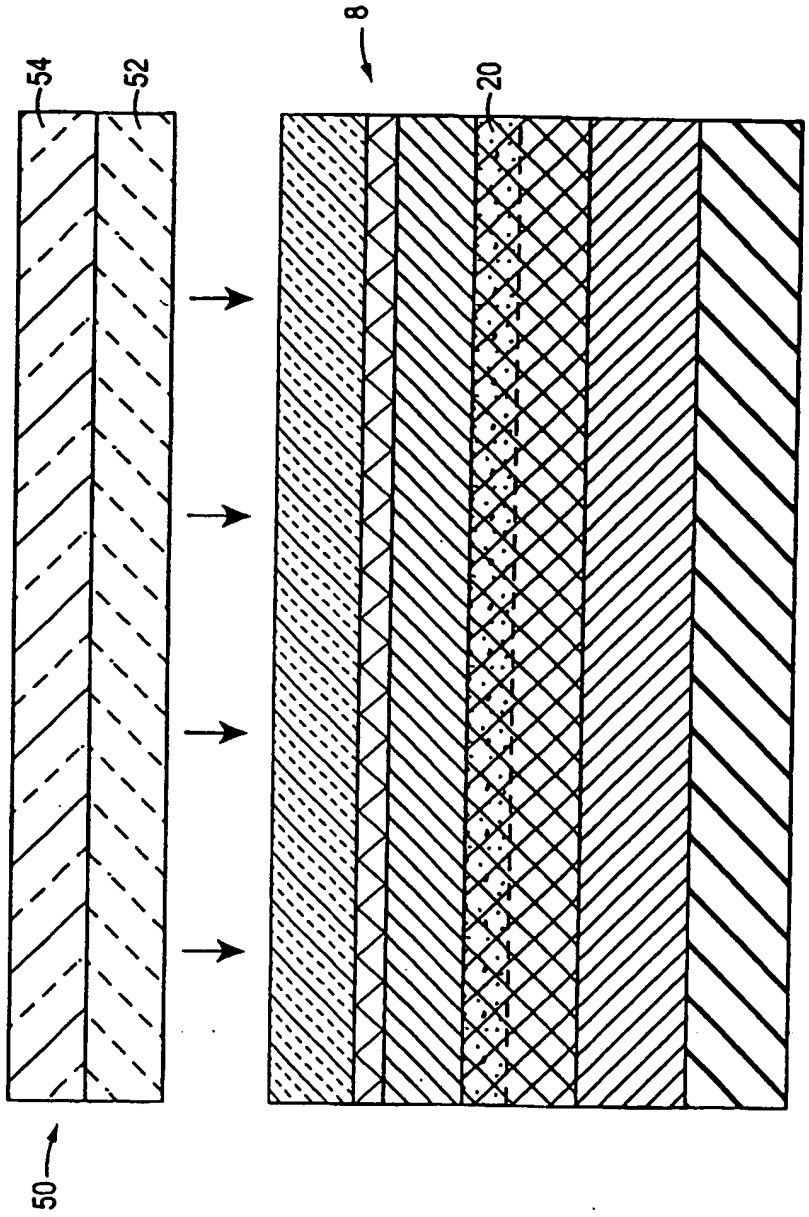

FIG. 24

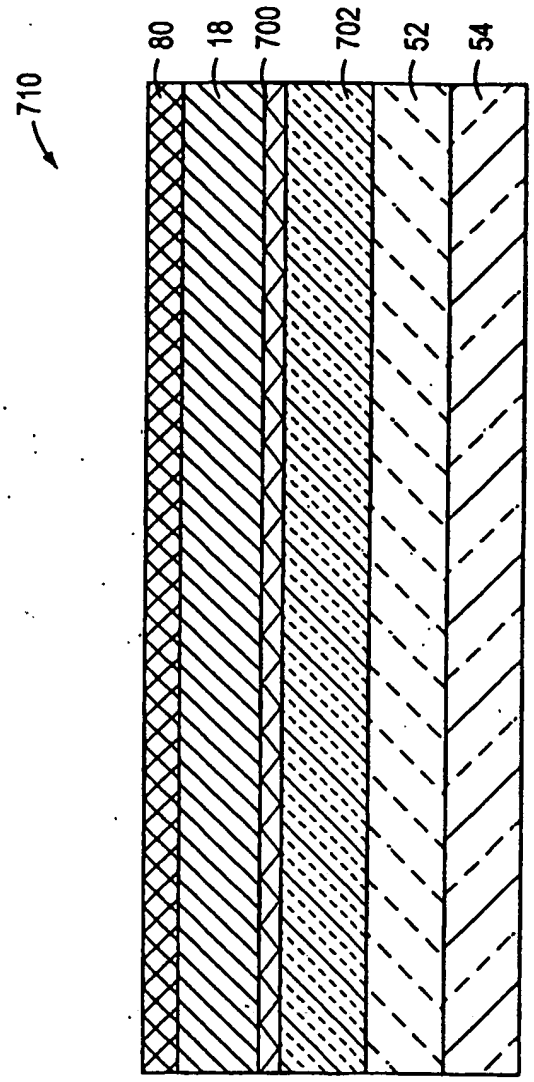

FIG. 25

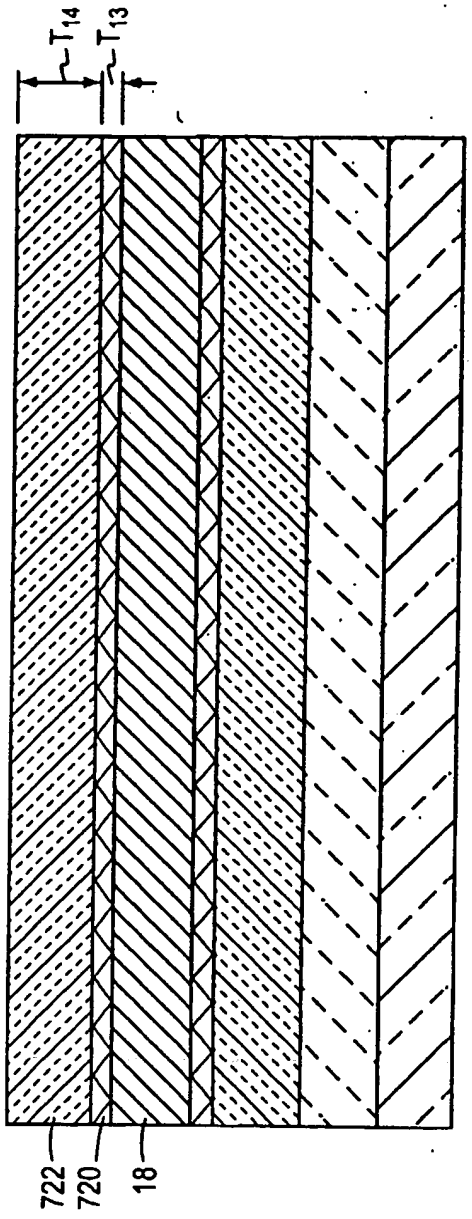

FIG. 26

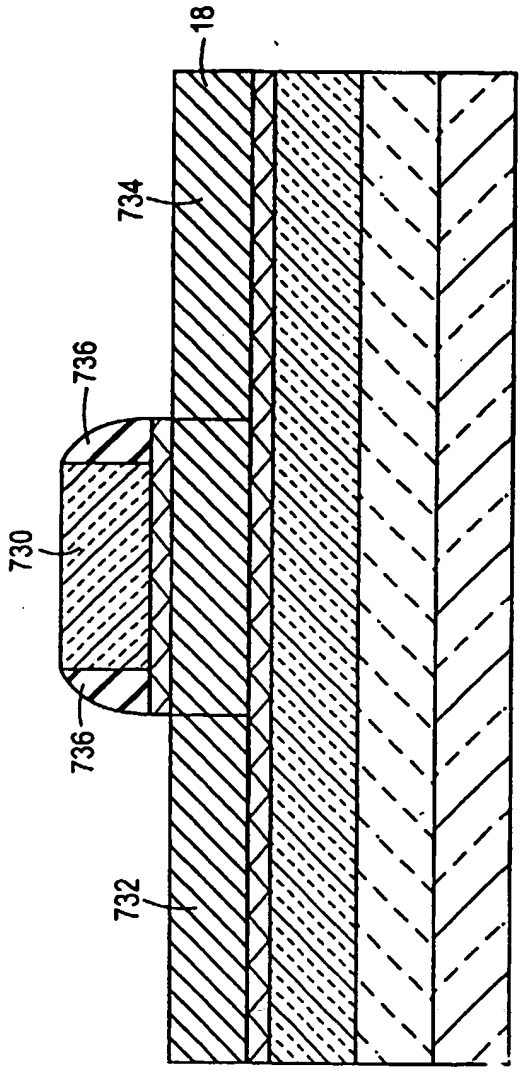

FIG. 27

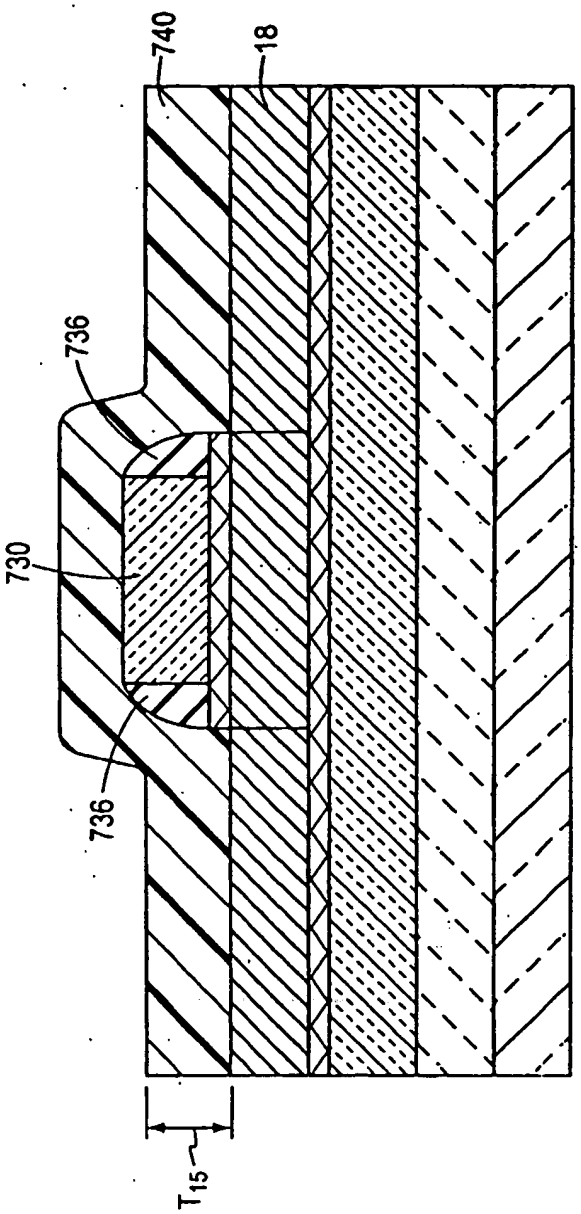

FIG. 28

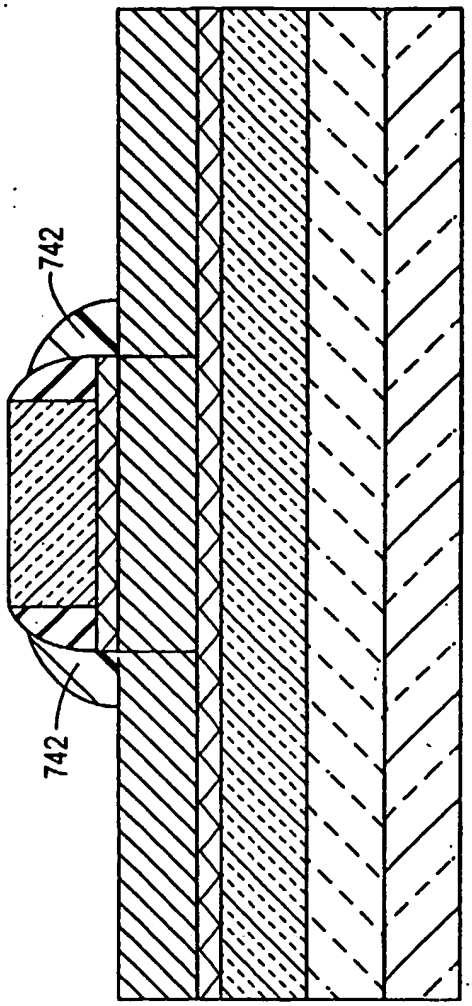

FIG. 29

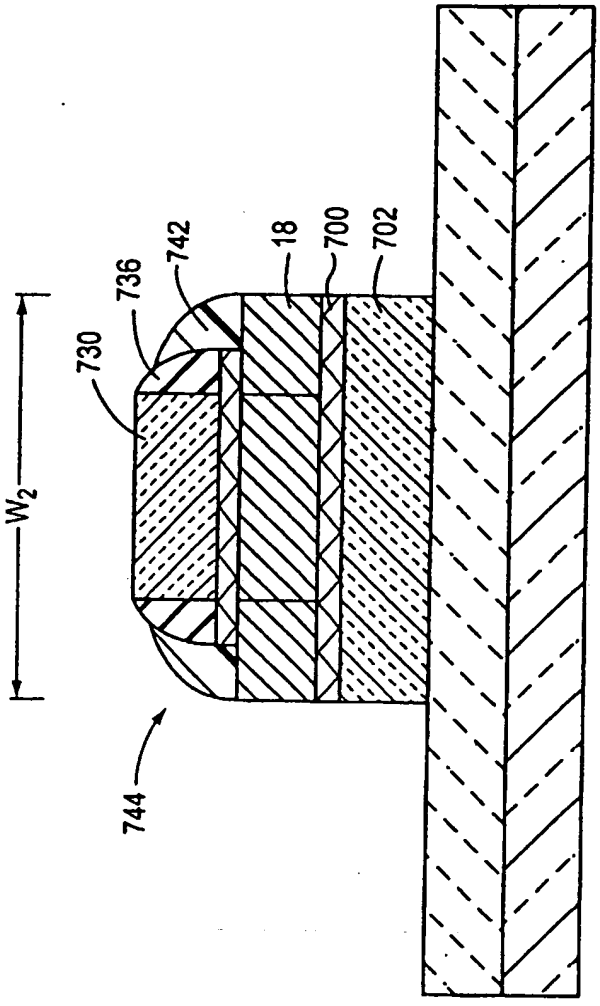

FIG. 30

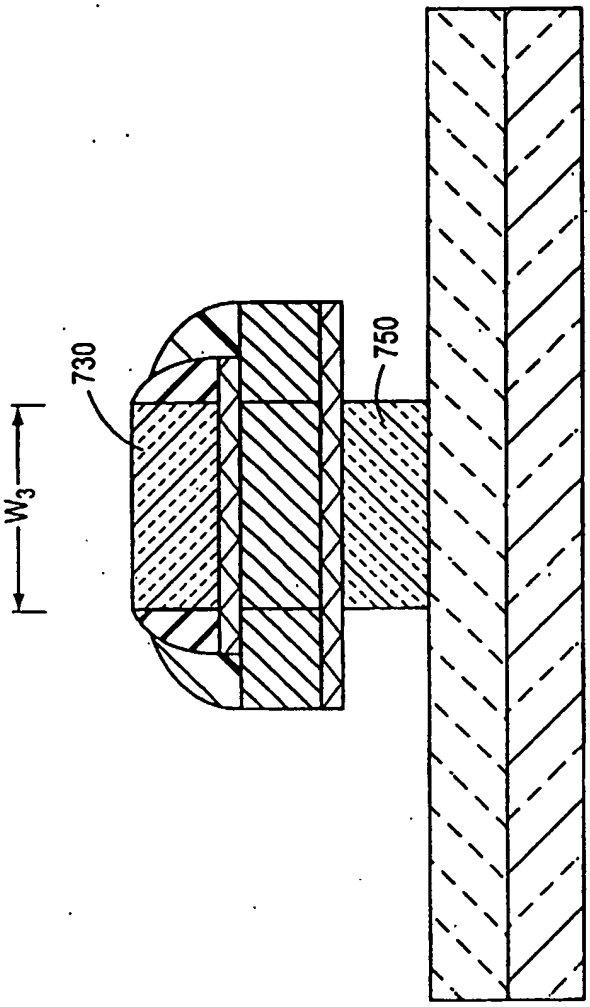

FIG. 31

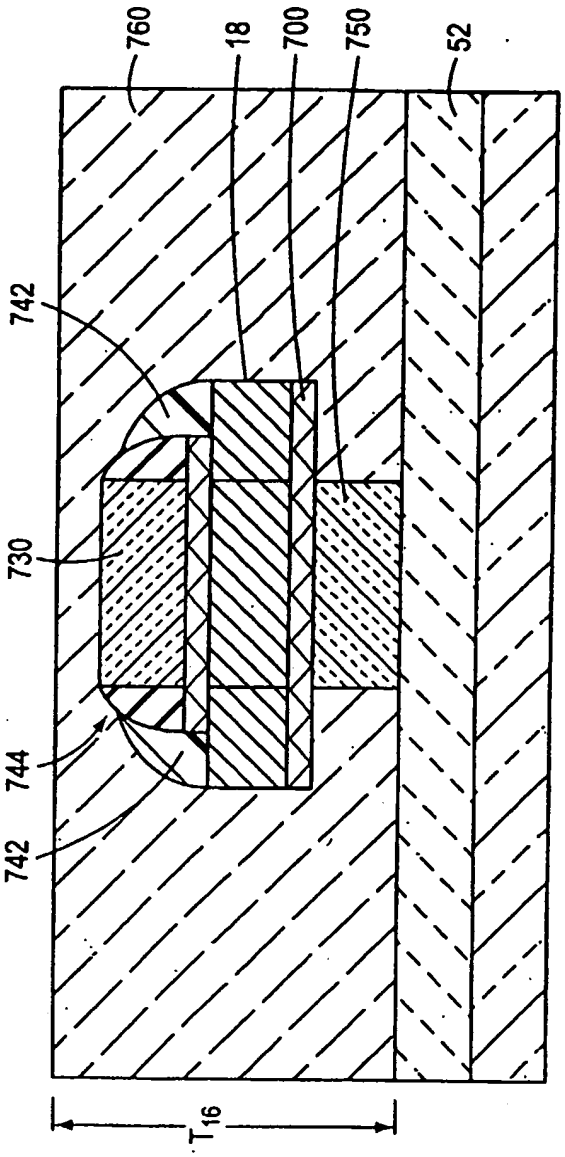

FIG. 32

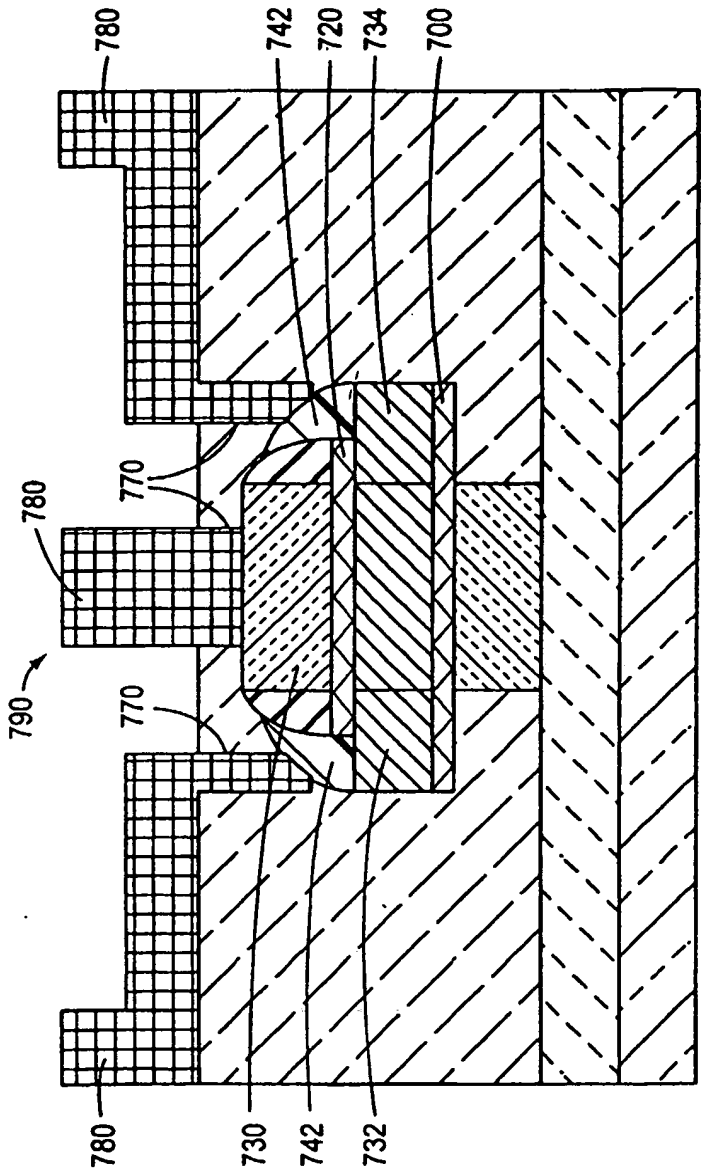

FIG. 33

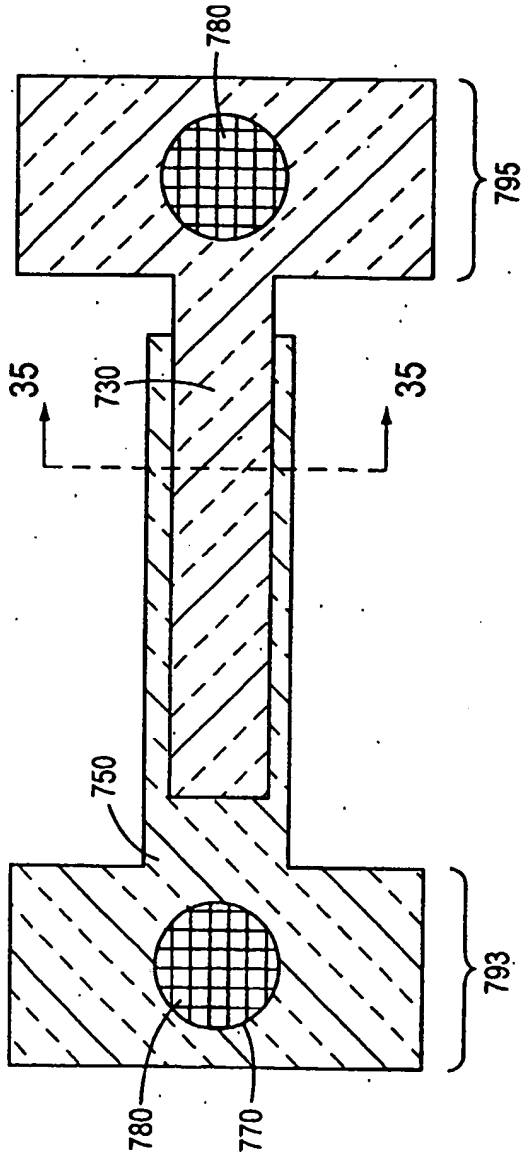

FIG. 34

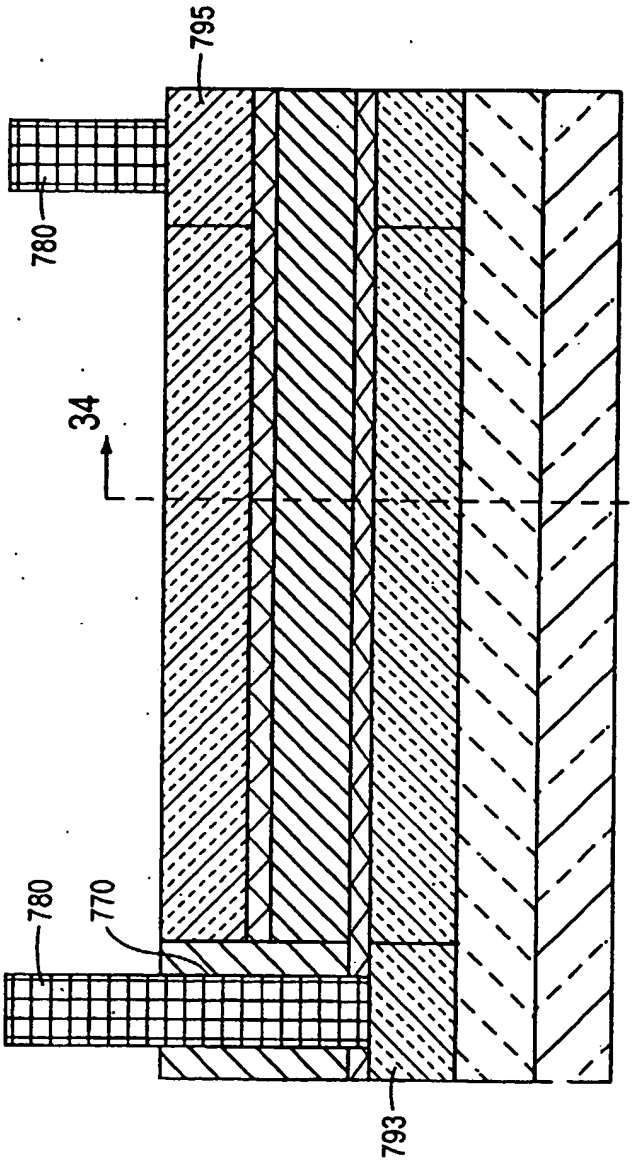

FIG. 35

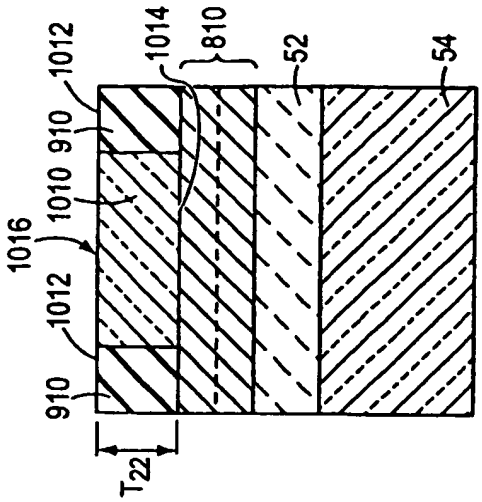

FIG. 38

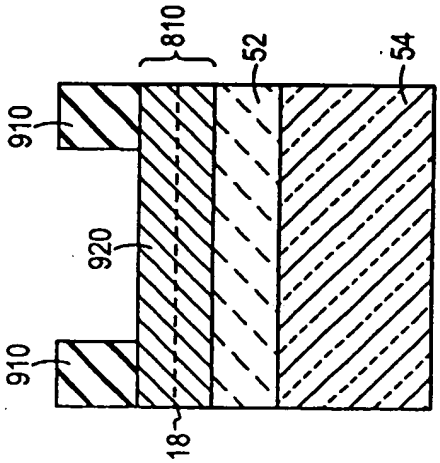

FIG. 37

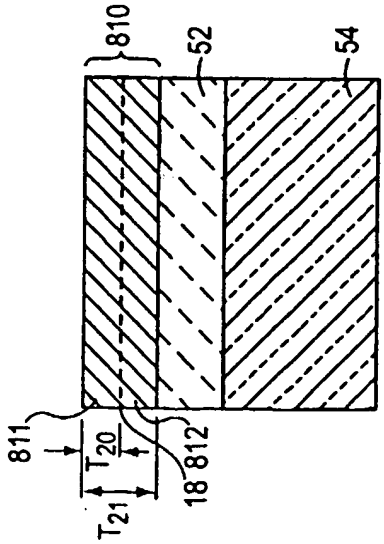

FIG. 36

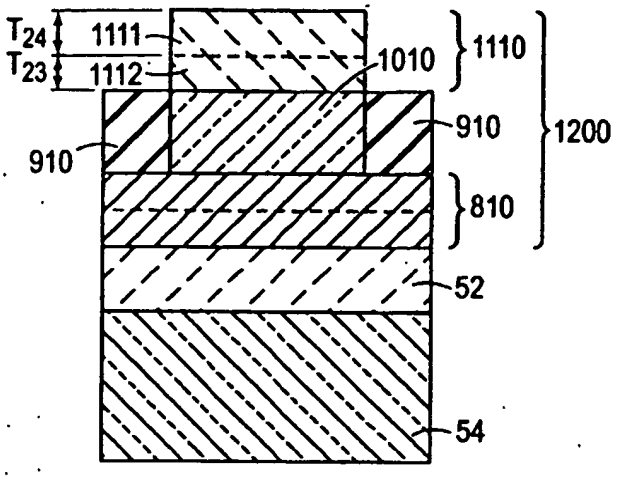

FIG. 39

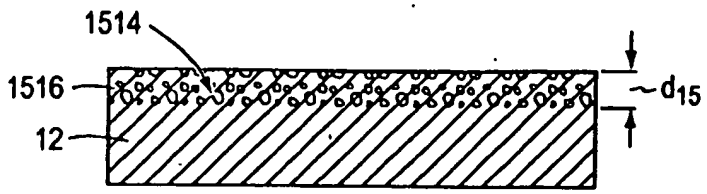

FIG. 40A

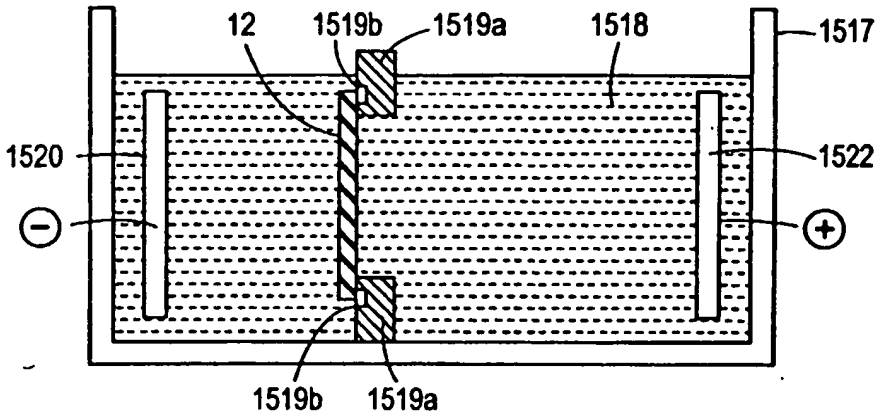

FIG. 40B

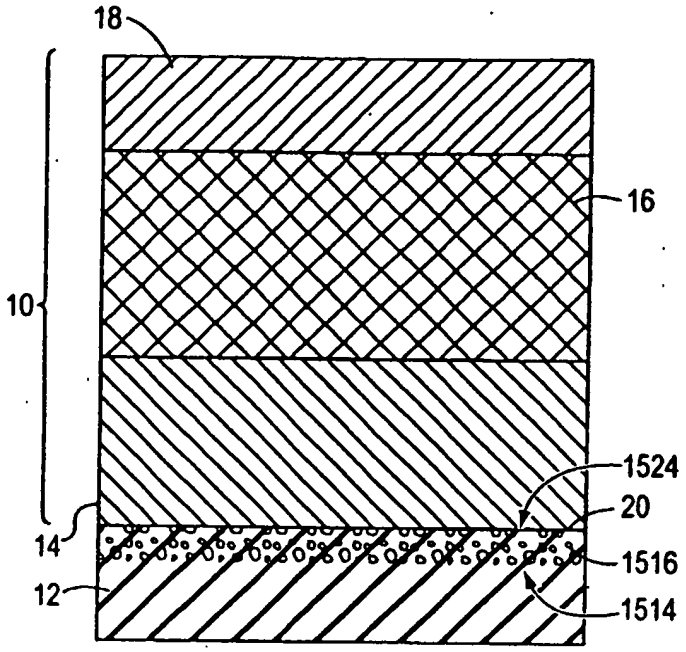

FIG. 40C

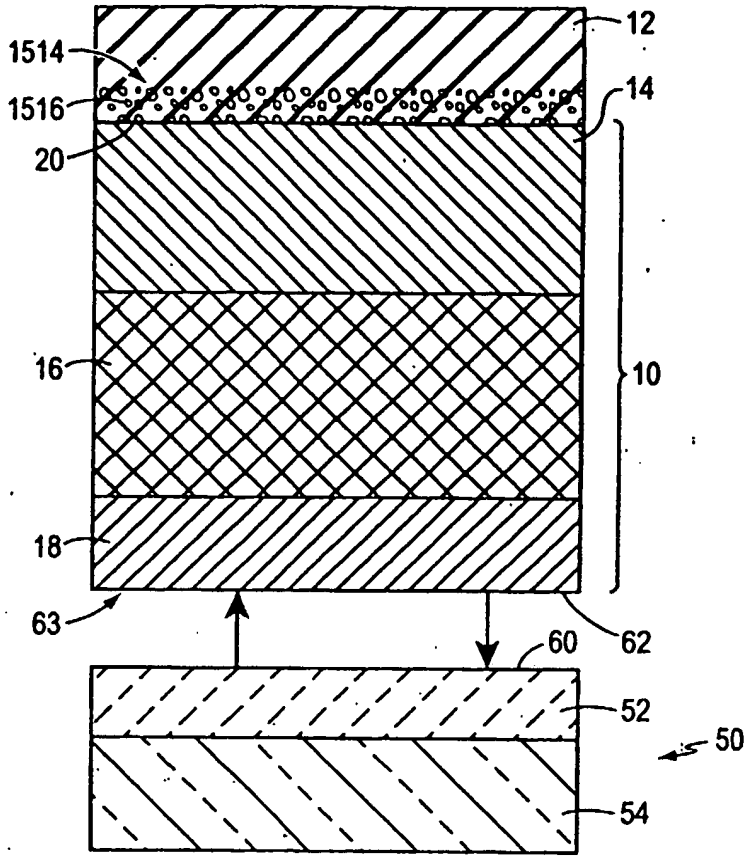

FIG. 40D

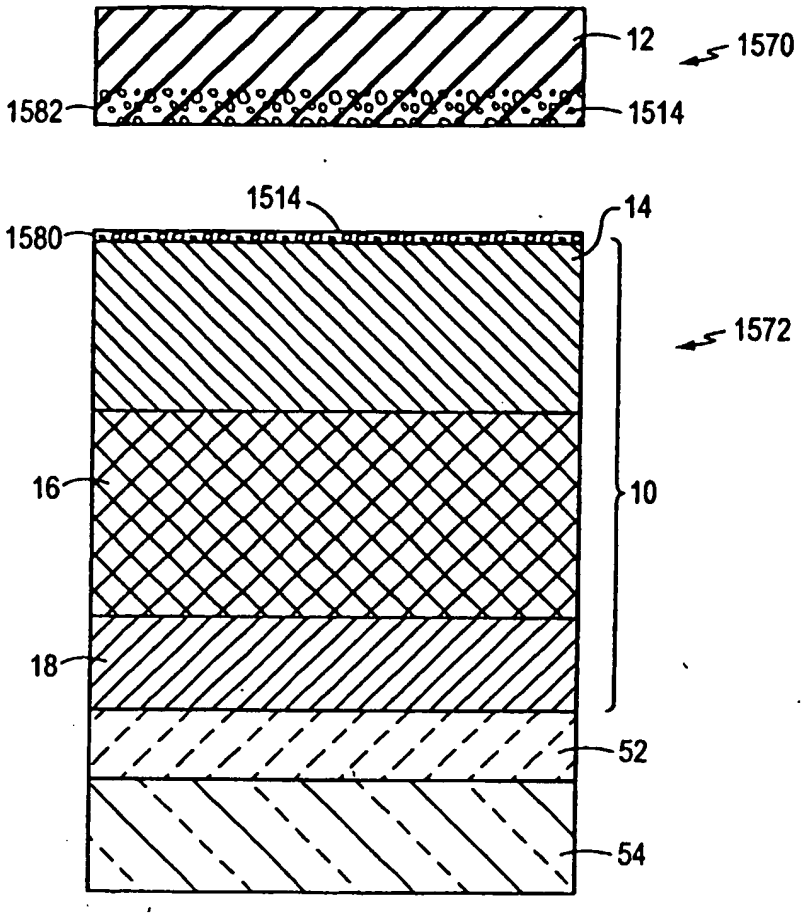

FIG. 40E

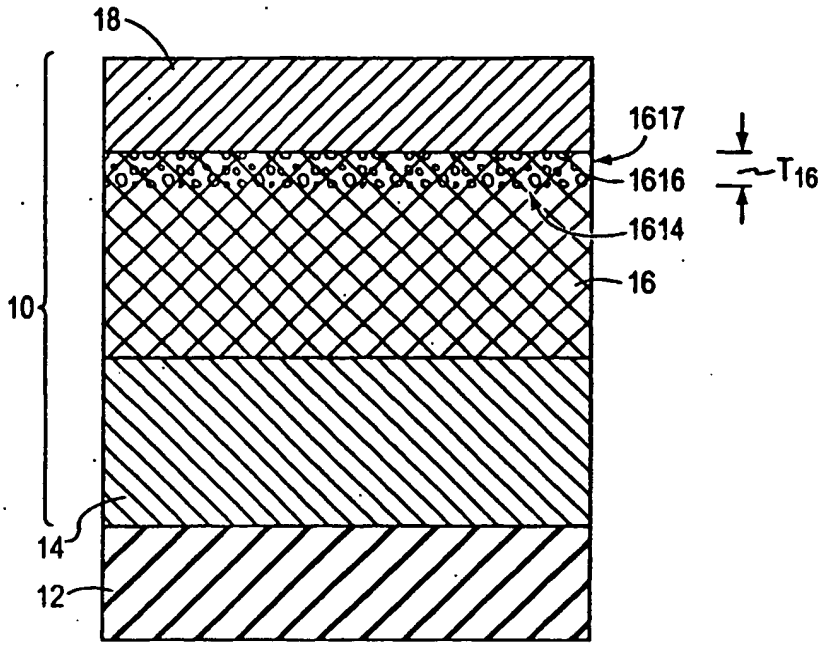

FIG. 41A

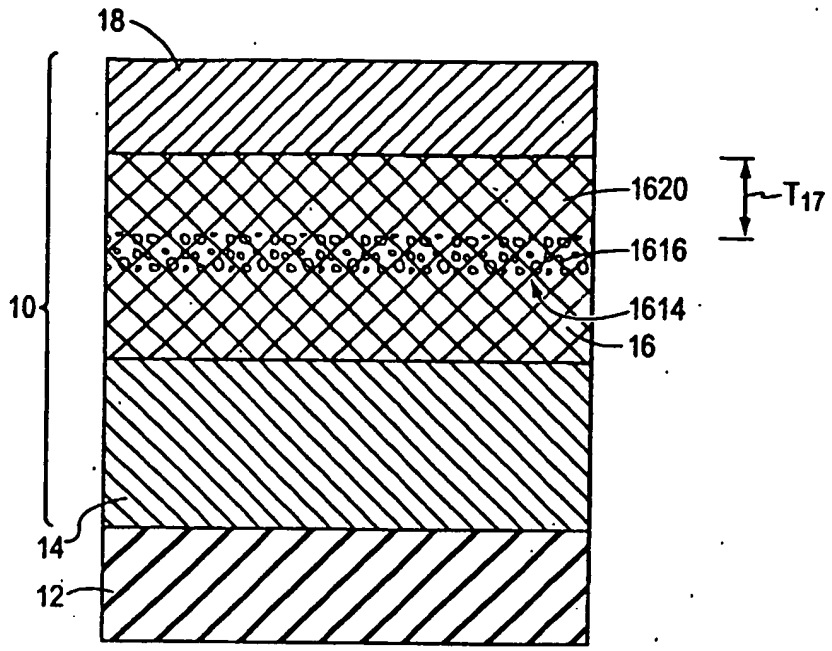

FIG. 41B

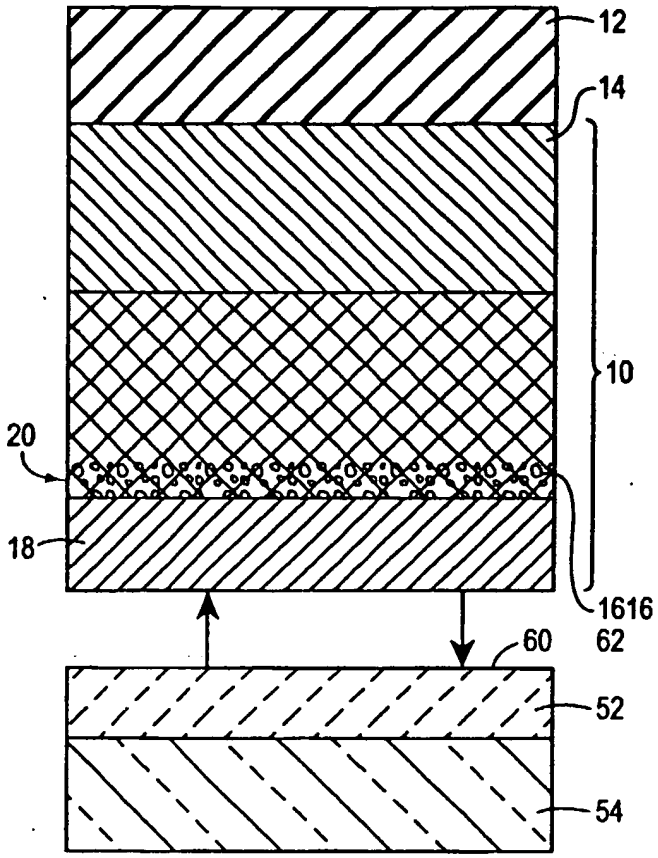

FIG. 41C

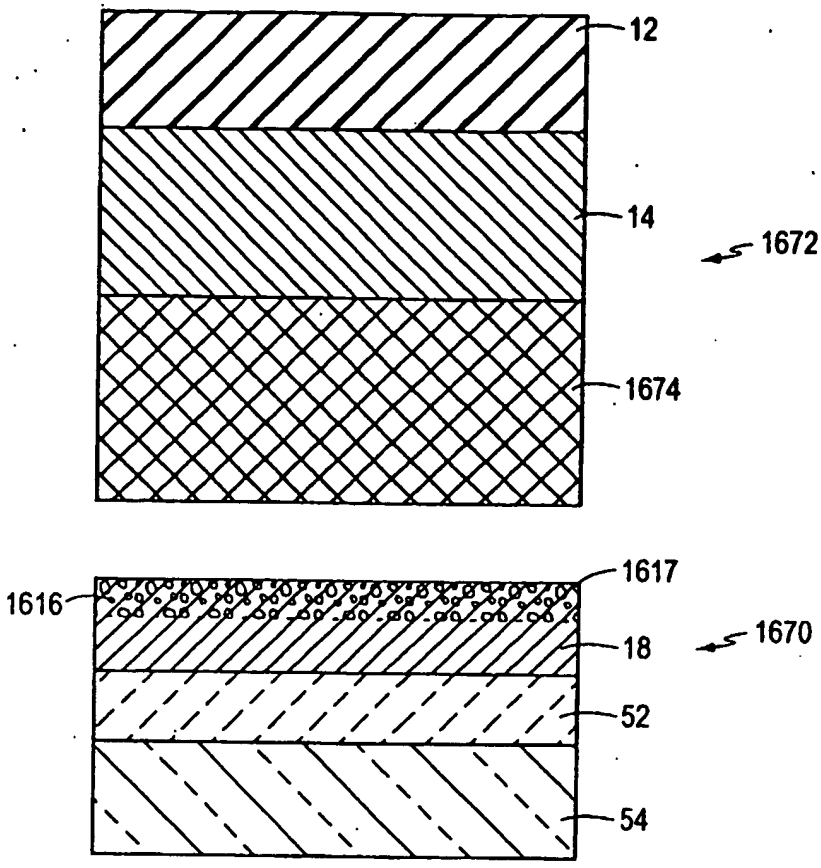

FIG. 41D

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
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18 December 2003 (18.12.2003)

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(30) Priority Data:

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60/404,058	15 August 2002 (15.08.2002)	US
60/416,000	4 October 2002 (04.10.2002)	US
10/264,935	4 October 2002 (04.10.2002)	US

(71) Applicant: AMBERWAVE SYSTEMS CORPORATION [US/US]; 13 Garabedian Drive, Salem, NH 03079 (US).

(72) Inventors: LOCHTEFELD, Anthony, J.; 73 Garrison Avenue, Somerville, MA 02144 (US). LANGDO, Thomas, A.; 195 Binney Street, Apt. 4302, Cambridge, MA 02142 (US). HAMMOND, Richard; 55 Sands Road, Harriseahead, Stoke-on-Trent, Staffordshire England ST74JZ (GB). CURRIE, Matthew, T.; 8 Fletcher Road, Windham, NH 03087 (US). BRAITHWAITE, Glyn; 1465 Hooksett Road, #186, Hooksett, NH 03106 (US). FITZGERALD, Eugene, A.; 7 Camelot Road, Windham, NH 03087 (US).

(74) Agent: NATASHA, C.; Testa, Hurwitz & Thibeault, LLP, High Street Tower, 125 High Street, Boston, MA 02110 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

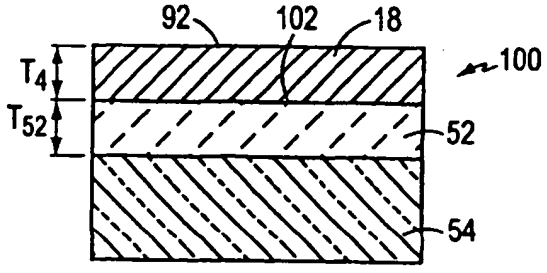
Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report: 4 March 2004

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 2003/105189 A3

(54) Title: STRAINED-SEMICONDUCTOR-ON-INSULATOR DEVICE STRUCTURES



(57) Abstract: The benefits of strained semiconductors are combined with silicon-on-insulator approaches to substrate and device fabrication.

INTERNATIONAL SEARCH REPORT

Application No
PCT/US 03/18007

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/762 H01L21/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 323 108 B1 (HOBART KARL D ET AL) 27 November 2001 (2001-11-27) column 3, line 42-53 column 5, line 11 -column 6, line 54 figure 1	
A	US 5 240 876 A (GAUL STEPHEN J ET AL) 31 August 1993 (1993-08-31) column 2, line 40 -column 3, line 9 figures 3A-3D	
A	US 5 013 681 A (KUB FRANCIS J ET AL) 7 May 1991 (1991-05-07) column 3, line 24 -column 5, line 5 figures 1-6	

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 December 2003	05/01/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Ekoué, A

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 02 15244 A (CHENG ZHI YUAN) 21 February 2002 (2002-02-21) claims 1-3	
P,A	LANGDO T. A., LOCHTEFELD A. ET AL.: "Preparation of Novel SiGe-free Strained Si on Insulator Substrates" IEEE INTERNATIONAL SOI CONFERENCE, 7 - 10 October 2002, pages 211-212, XP002263057 the whole document	
P,A	US 2003/003679 A1 (DOYLE BRIAN S ET AL) 2 January 2003 (2003-01-02) paragraph '0021!	
P,A	US 2002/140031 A1 (RIM KERN) 3 October 2002 (2002-10-03) page 2, paragraphs 12-15	
A	US 6 372 593 B1 (HATTORI NOBUYOSHI ET AL) 16 April 2002 (2002-04-16) column 8, line 18 -column 9, line 4 figure 3	
A	GODBEY D J ET AL: "FABRICATION OF BOND AND ETCH-BACK SILICON INSULATOR USING A STRAINED SI0.7GE0.3 LAYER AS AN ETCH STOP" JOURNAL OF THE ELECTROCHEMICAL SOCIETY, ELECTROCHEMICAL SOCIETY. MANCHESTER, NEW HAMPSHIRE, US, vol. 137, no. 10, October 1990 (1990-10), pages 3219-3223, XP000159775 ISSN: 0013-4651 the whole document	
A	HUANG L-J ET AL: "Carrier mobility enhancement in strained Si-on-insulatoir fabricated by wafer bonding" 2001 SYMPOSIUM ON VLSI TECHNOLOGY. DIGEST OF TECHNICAL PAPERS. KYOTO, JAPAN, JUNE 12 - 14, 2001, SYMPOSIUM ON VLSI TECHNOLOGY, TOKYO: JSAP, JP, 12 June 2001 (2001-06-12), pages 57-58, XP010551998 ISBN: 4-89114-012-7 the whole document	

INTERNATIONAL SEARCH REPORT

Inter nal application No.
PCT/US 03/18007

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 1-202
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box I.2

Claims Nos.: 1-202

In view of the large number and also the wording of the claims presently on file, which render it difficult, if not impossible, to determine the matter for which protection is sought, the present application fails to comply with the clarity and conciseness requirements of Article 6 PCT (see also Rule 6.1(a) PCT) to such an extent that a meaningful search is impossible. Consequently, the search has been carried out for those parts of the application which do appear to be clear (and concise), namely: (see page 4, lines 6-8; page 5, lines 27-31; page 18, lines 9-11)

- a structure that includes a first substrate having a dielectric layer disposed thereon, and a first Si1-xGex strained layer disposed in contact with the dielectric;

- a method for forming a structure, the method including providing a first substrate having a first Si1-xGex strained layer formed thereon, bonding the first strained semiconductor layer to an insulator layer disposed on a second substrate and, removing the first substrate from the first Si1-xGex strained layer, the strained Si1-xGex layer remaining bonded to the insulator layer".

(As it is said in the description of the present application, the other features of the structure and the method may just be included)

The applicant's attention is drawn to the fact that claims, or parts of claims, relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.

INTERNA ..NAL SEARCH REPORT

In...ation on patent family members

In...atl Application No
PCT/US 03/18007

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6323108 B1	27-11-2001	NONE	
US 5240876 A	31-08-1993	US 5218213 A	08-06-1993
US 5013681 A	07-05-1991	CA 2066193 A1	30-03-1991
		EP 0493503 A1	08-07-1992
		JP 2684455 B2	03-12-1997
		JP 4506587 T	12-11-1992
		KR 9506967 B1	26-06-1995
		WO 9105366 A1	18-04-1991
WO 0215244 A	21-02-2002	EP 1309989 A2	14-05-2003
		WO 0215244 A2	21-02-2002
		US 2003155568 A1	21-08-2003
		US 2003168654 A1	11-09-2003
		US 2002072130 A1	13-06-2002
US 2003003679 A1	02-01-2003	NONE	
US 2002140031 A1	03-10-2002	WO 02080241 A1	10-10-2002
US 6372593 B1	16-04-2002	JP 2001036054 A	09-02-2001
		FR 2796757 A1	26-01-2001
		US 2002019105 A1	14-02-2002

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(19) World Intellectual Property Organization
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(10) International Publication Number
WO 2003/105189 A3

(51) International Patent Classification[7]: H01L 21/762, 21/20

(21) International Application Number: PCT/US2003/018007

(22) International Filing Date: 6 June 2003 (06.06.2003)

(25) Filing Language: English

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(30) Priority Data:

60/386,968	7 June 2002 (07.06.2002)	US
60/404,058	15 August 2002 (15.08.2002)	US
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(71) Applicant: AMBERWAVE SYSTEMS CORPORATION [US/US]; 13 Garabedian Drive, Salem, NH 03079 (US).

(72) Inventors: LOCHTEFELD, Anthony, J.; 73 Garrison Avenue, Somerville, MA 02144 (US). LANGDO, Thomas, A.; 195 Binney Street, Apt. 4302, Cambridge, MA 02142 (US). HAMMOND, Richard; 55 Sands Road, Harriseahead, Stoke-on-Trent, Staffordshire England ST74JZ (GB). CURRIE, Matthew, T.; 8 Fletcher Road, Windham, NH 03087 (US). BRAITHWAITE, Glyn; 1465 Hooksett Road, #186, Hooksett, NH 03106 (US). FITZGERALD, Eugene, A.; 7 Camelot Road, Windham, NH 03087 (US).

(74) Agent: NATASHA, C.; Testa, Hurwitz & Thibeault, LLP, High Street Tower, 125 High Street, Boston, MA 02110 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *with amended claims*

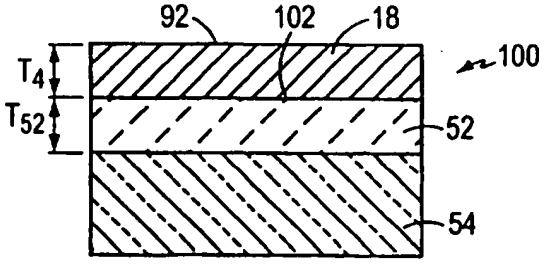
(88) Date of publication of the international search report: 4 March 2004

Date of publication of the amended claims: 21 May 2004

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 2003/105189 A3

(54) Title: STRAINED-SEMICONDUCTOR-ON-INSULATOR DEVICE STRUCTURES



(57) Abstract: The benefits of strained semiconductors are combined with silicon-on-insulator approaches to substrate and device fabrication.

AMENDED CLAIMS

[received by the International Bureau on 03 March 2004 (03.03.04);
claims 188-190, 192-193, 196-198 and 200-202 are replaced by amended claims,
claims 1-187, 191, 194-195 and 199 remain unchanged]

187. A method for forming a structure, the method comprising:

providing a substrate having a strained semiconductor layer disposed over a dielectric layer;

defining a collector in a portion of the strained semiconductor layer;

forming a base over the collector; and

forming an emitter over the base.

188. The method of claim 187, wherein the strained semiconductor layer is tensilely strained.

189. The method of claim 188, wherein the strained semiconductor layer comprises tensilely strained silicon.

190. The method of claim 187, wherein the strained semiconductor layer is compressively strained.

191. A method for forming a structure, the method comprising:

providing a first substrate having a strained layer disposed thereon, wherein the strained layer includes a first semiconductor material;

bonding the strained layer to a second substrate, wherein the second substrate comprises a bulk material;

removing the first substrate from the strained layer, the strained layer remaining bonded to the bulk semiconductor material;

defining a collector in a portion of the strained layer;

forming a base over the collector; and

forming an emitter over the base,

wherein the strain of the strained layer is not induced by the second substrate and the strain is independent of lattice mismatch between the strained layer and the second substrate.

192. The method of claim 191, wherein the strained layer is tensilely strained.

193. The method of claim 192 wherein the strained layer comprises tensilely strained silicon.

194. The method of claim 187 wherein the strained layer is compressively strained.

195. A method for forming a structure, the method comprising:

providing a relaxed substrate comprising a bulk material and a strained layer disposed in contact with the relaxed substrate, the strain of the strained layer not being induced by the underlying substrate and the strain being independent of a lattice mismatch between the strained layer and the relaxed substrate;

defining a collector in a portion of the strained layer;

forming a base over the collector; and

forming an emitter over the base.

196. The method of claim 195, wherein the strained layer is tensilely strained.

197. The method of claim 196, wherein the strained layer comprises tensilely strained silicon.

198. The method of claim 195 wherein the strained layer is compressively strained.

199. A method for forming a structure, the method comprising:

providing a substrate having a strained semiconductor layer disposed over a substrate dielectric layer;

forming a transistor in the strained layer by

forming a gate dielectric layer above a portion of the strained semiconductor layer,

forming a gate contact above the gate dielectric layer, and

forming a source region and a drain region in a portion of the strained semiconductor layer, proximate the gate dielectric layer;

removing a portion of the strained layer and the substrate dielectric layer to expose a portion of the substrate;

defining a collector in the exposed portion of the substrate;

forming a base over the collector; and

forming an emitter over the base.

200. The method of claim 199, wherein the strained layer is tensilely strained.

201. The method of claim 200, wherein the strained layer comprises tensilely strained silicon.

202. The method of claim 199, wherein the strained layer is compressively strained.